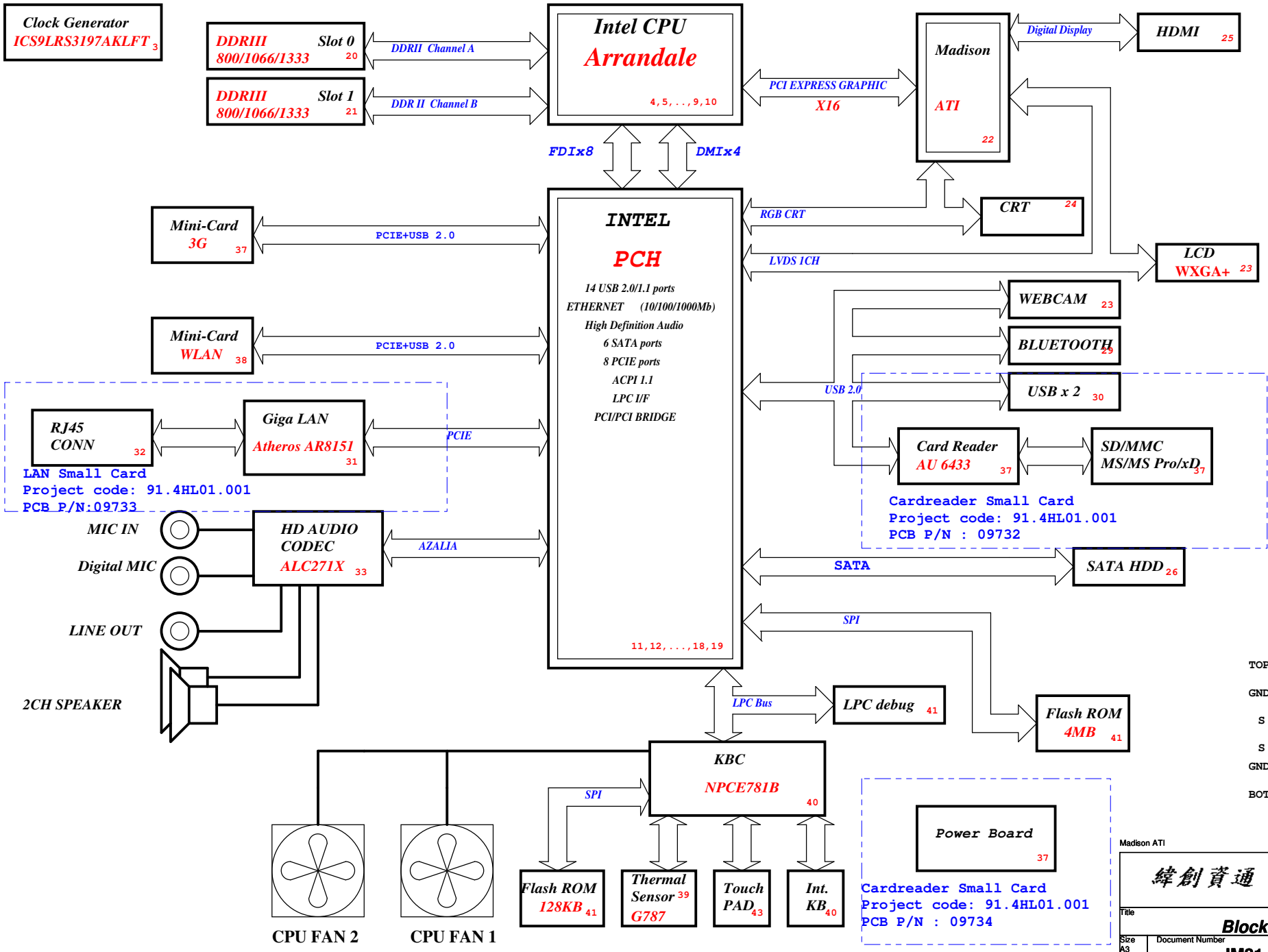
JM31-CP Block Diagram

Project code: 91.4HL01.001
PCB P/N : 48.4HL01.031
REVISION : 09921-3



SYSTEM DC/DC RT8223BGQW	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

CPU DC/DC ISL62882HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

MAXIM CHARGER ISL62881HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 53

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard1**
LANE3	**MiniCard2**

USB Table

Pair	*Device*
0	*USB1*
1	*USB2*
2	*USB4*
3	*MINICARD2*
4	*WECAM*
5	*Blue Tooth*
6	*MINIC1*
7	*Cardreader*
8	*NC*
9	*NC*
10	*NC*
11	*NC*
12	*NC*
13	*NC*

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Title: **Table of Content**

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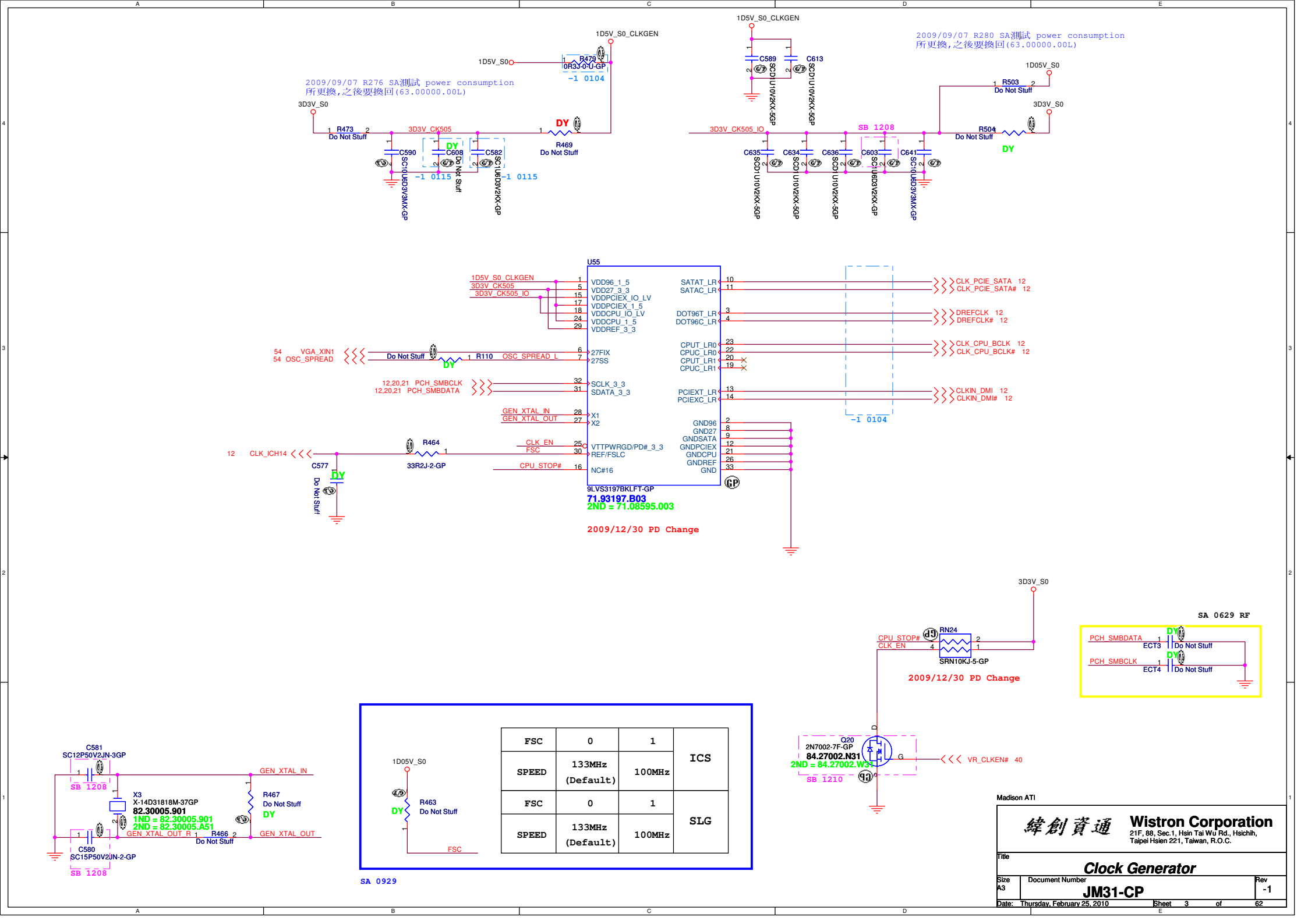
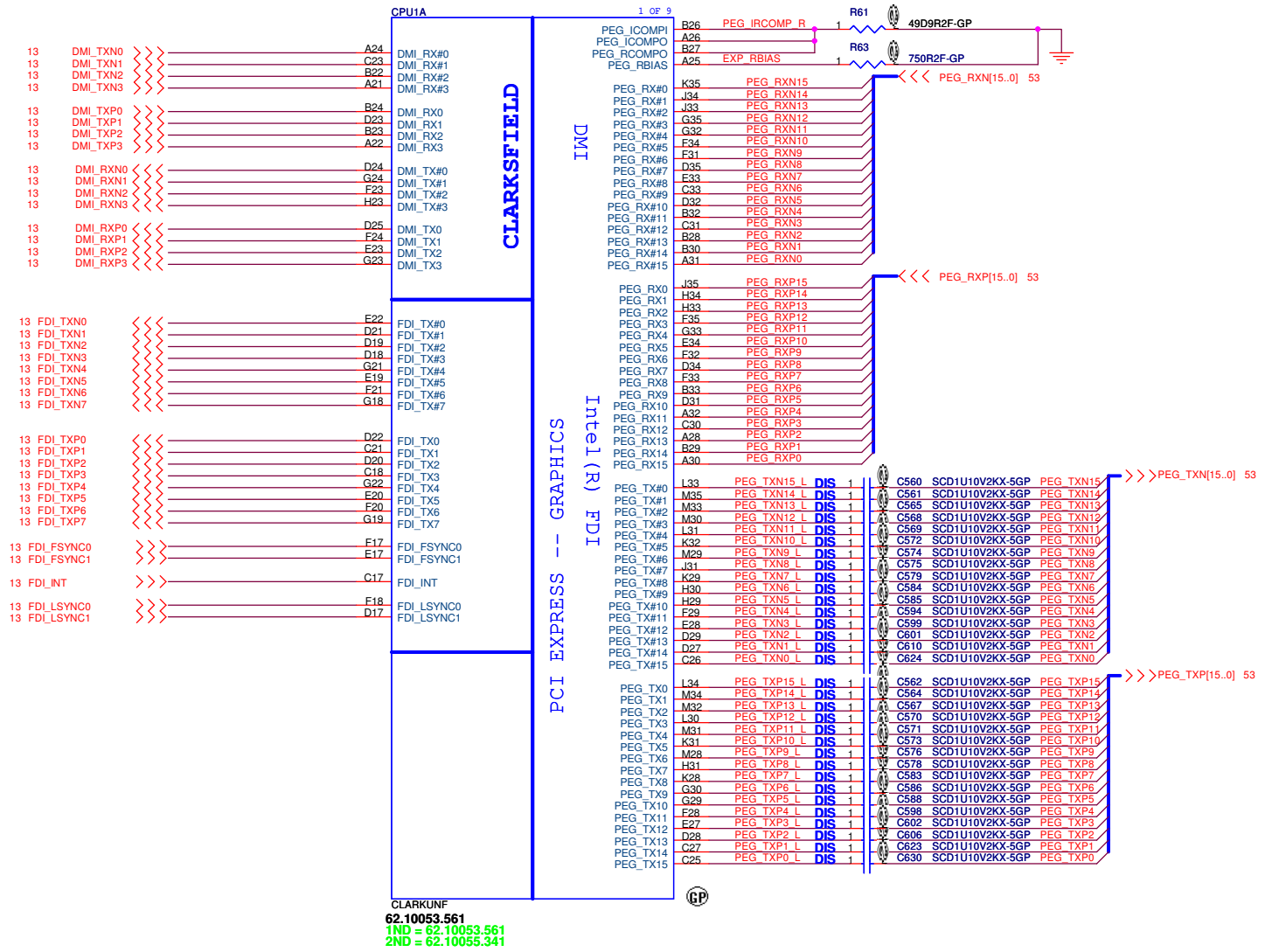


FSC	0	1	ICS
SPEED	133MHz (Default)	100MHz	
FSC	0	1	SLG
SPEED	133MHz (Default)	100MHz	



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Title: **CPU (1/7)**

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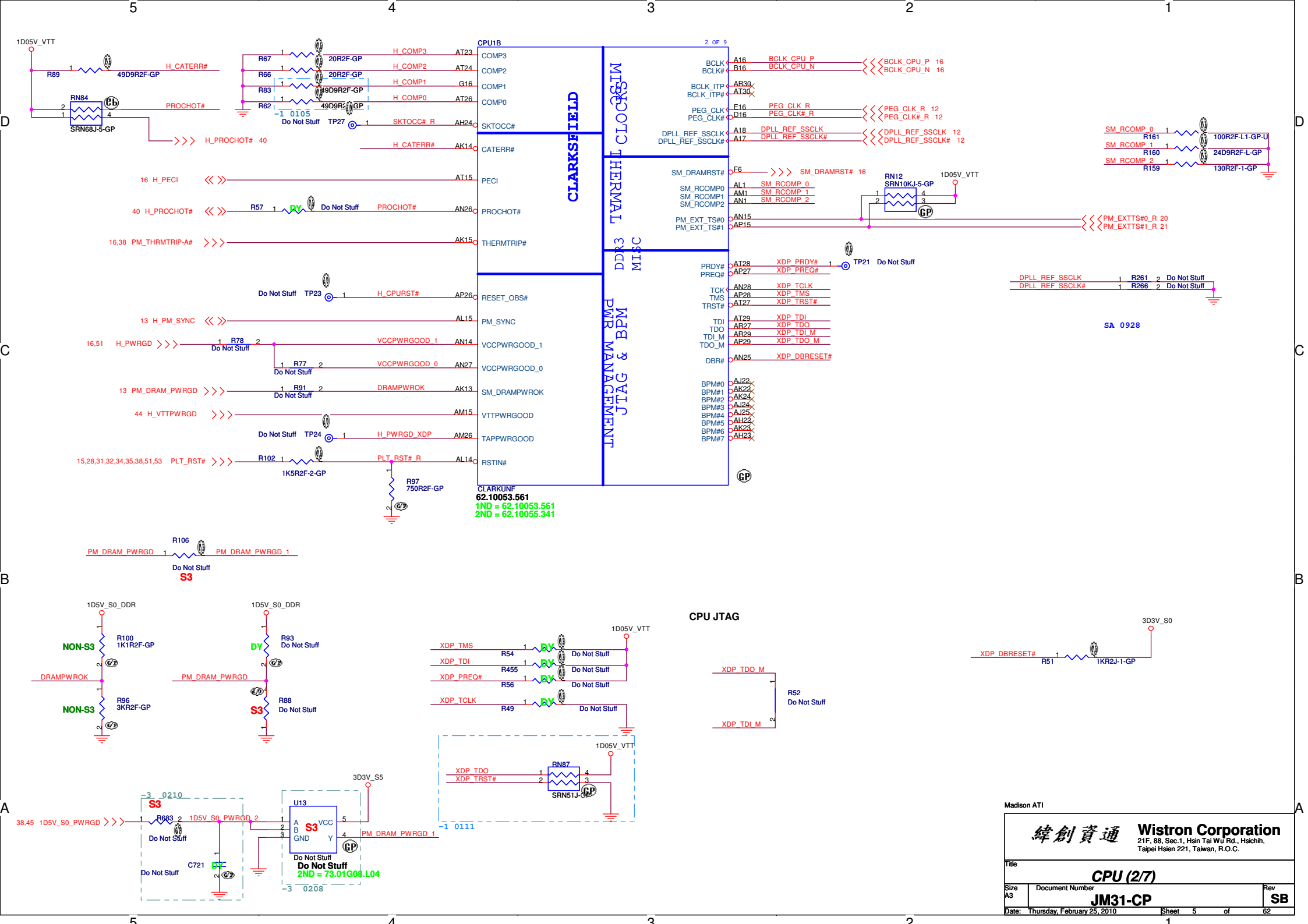
CPU1B
CLARKSFIELD
MISC THERMAL DDR3 MISC
JTAG & BPM PWR MANAGEMENT
2 OF 9
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
CPU JTAG
SA 0928
Do Not Stuff
S3
NON-S3
DY
GP
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Title
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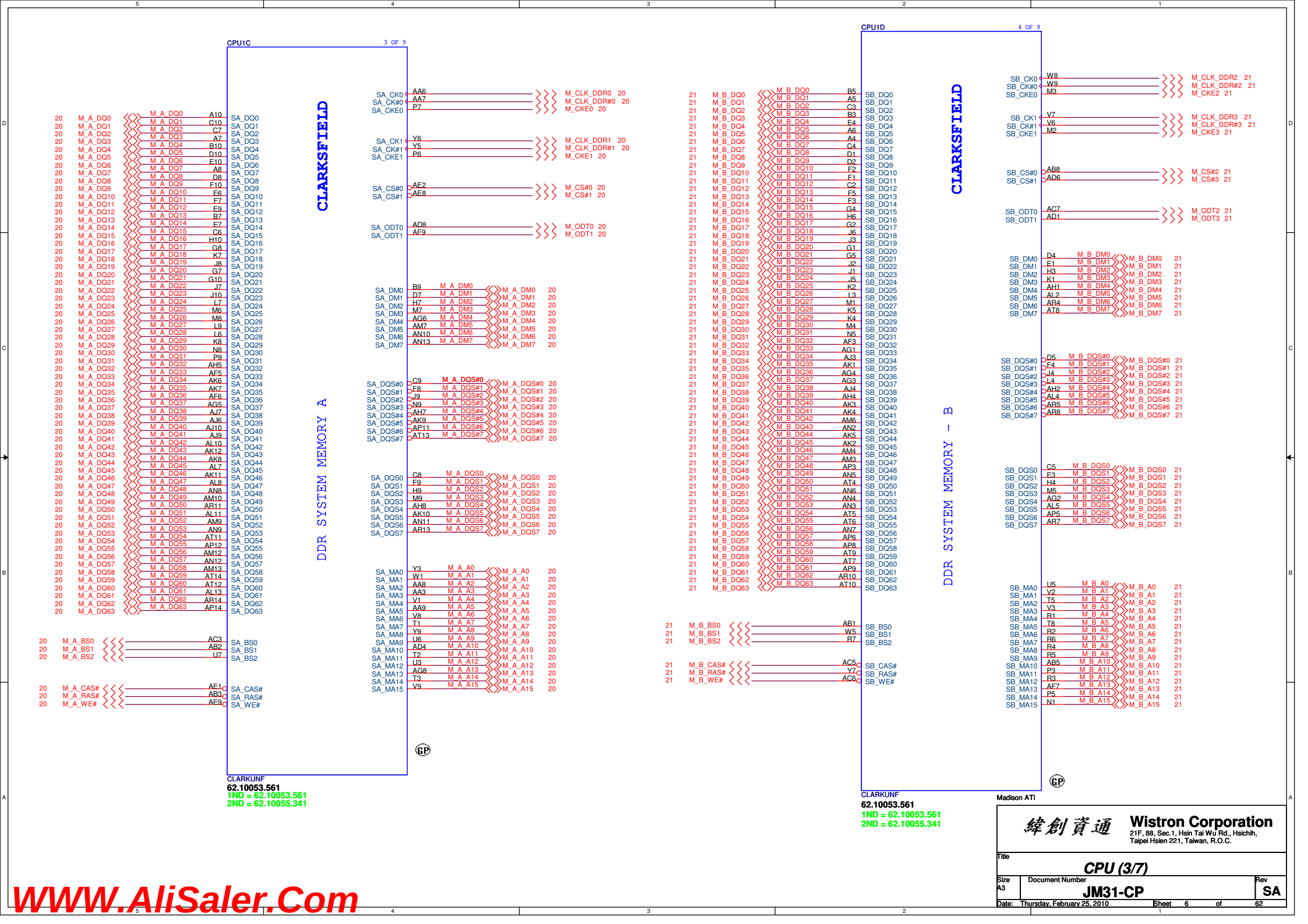

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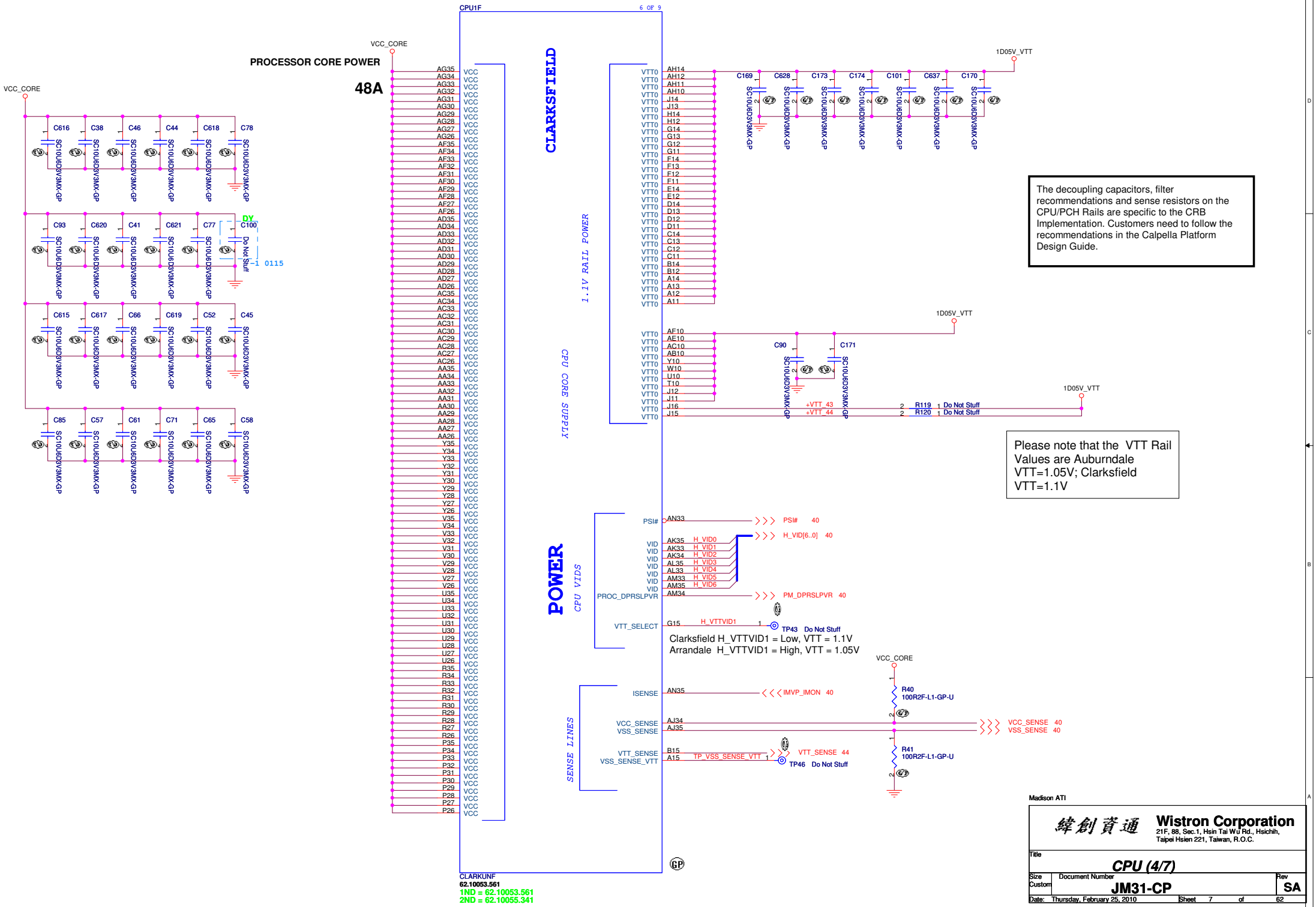
PROCESSOR CORE POWER
48A
VCC_CORE
CPU1F
6 OF 9
CLARKSFIELD
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
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Title
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Custom
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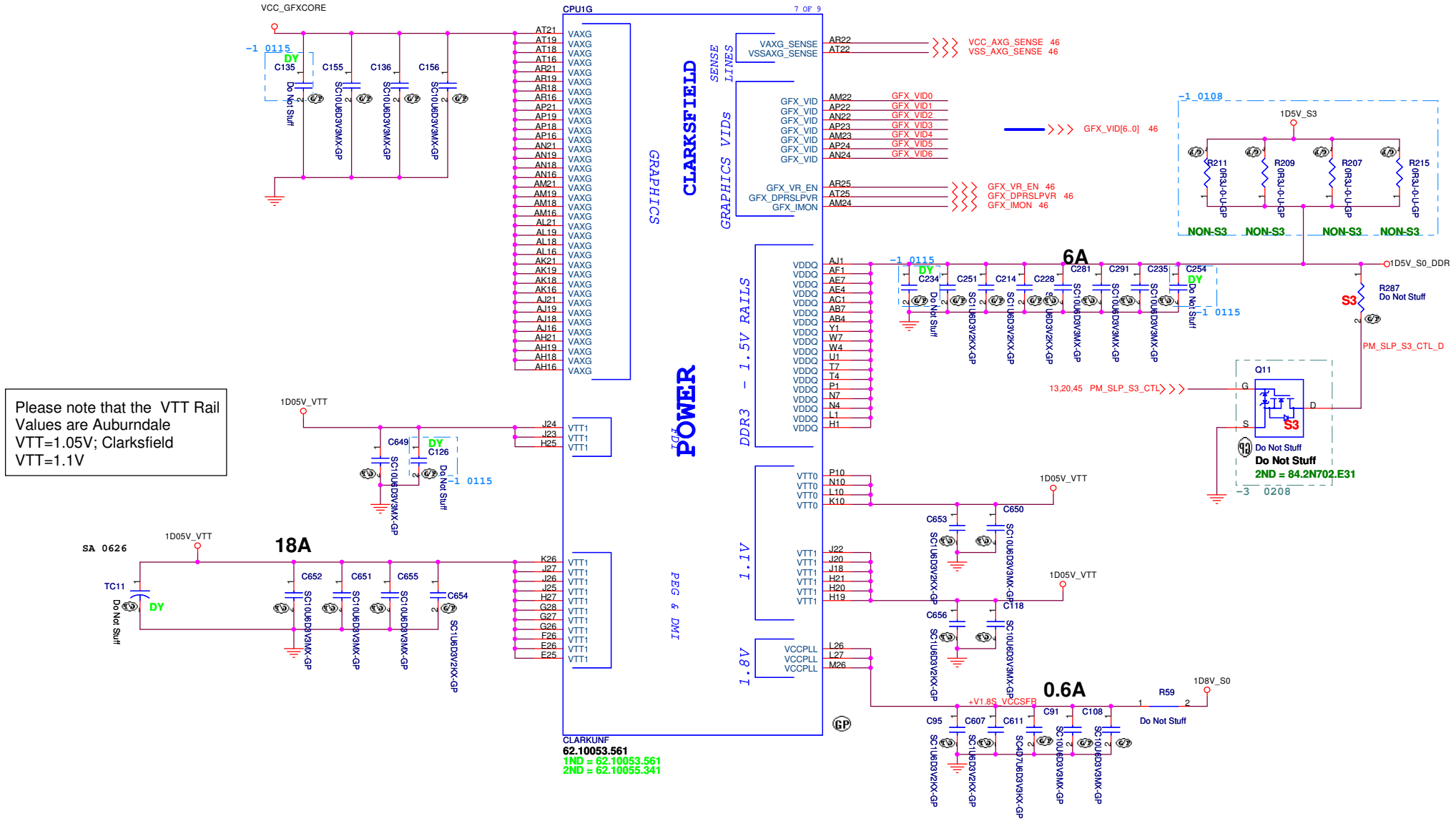

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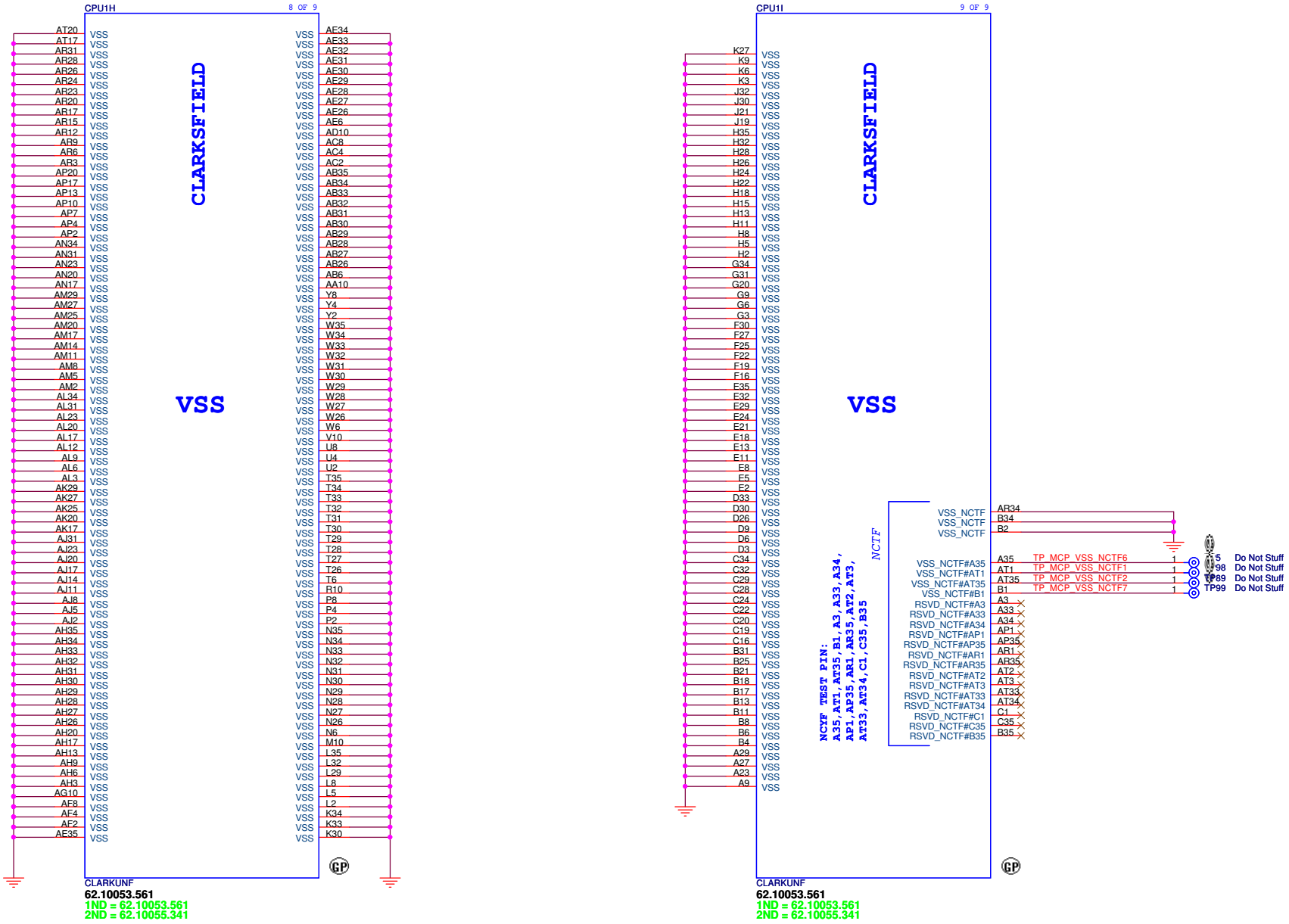

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Title: ***CPU (6/7)***

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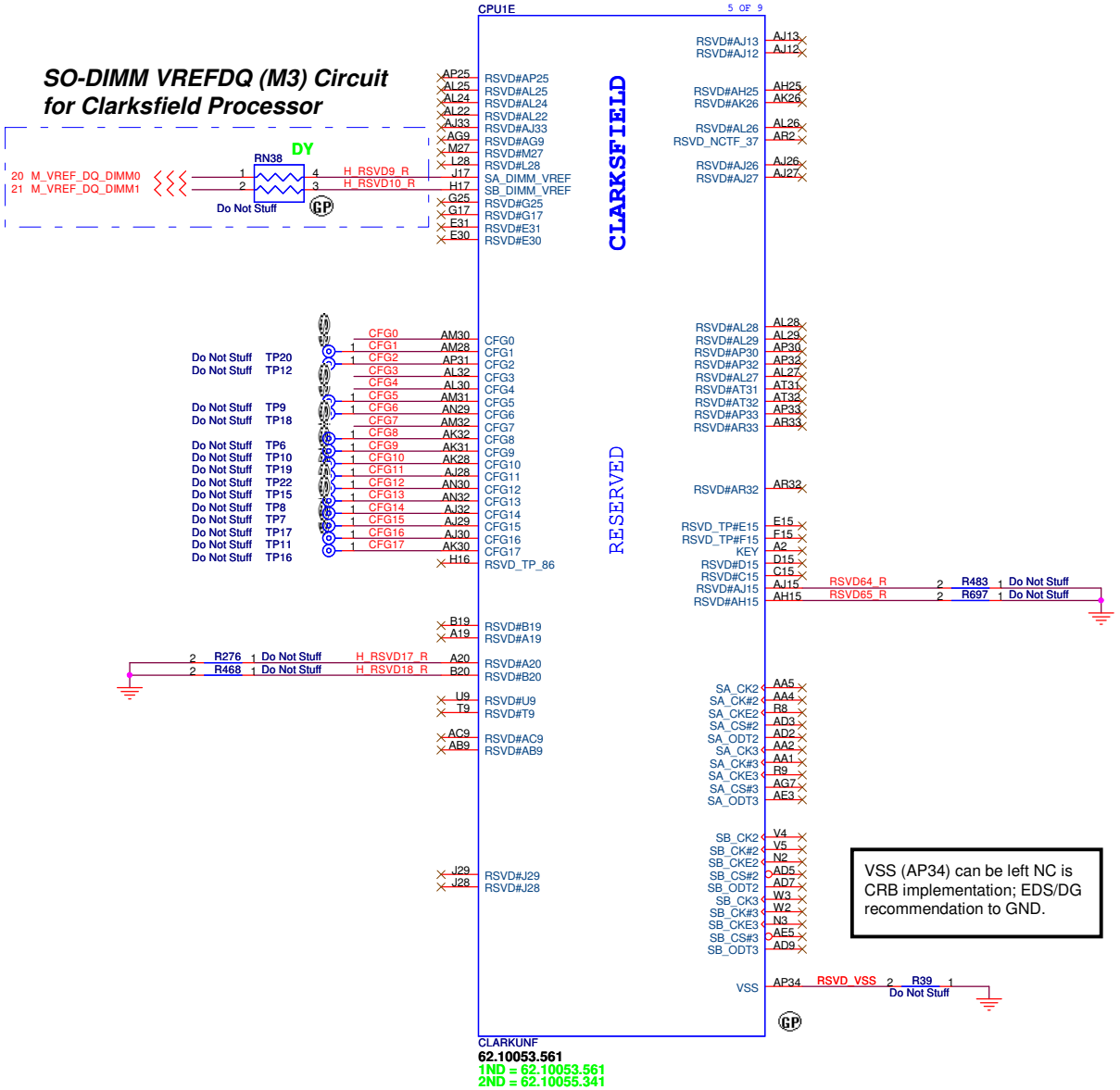
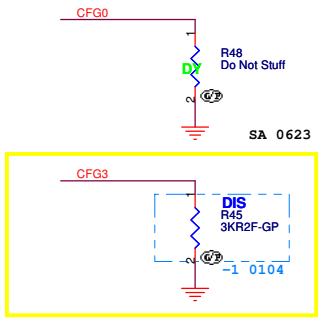
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709

When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

PCH1A — 1 OF 10

iBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002

SA 0629 RF

SA 1012

SA 0930

HDD

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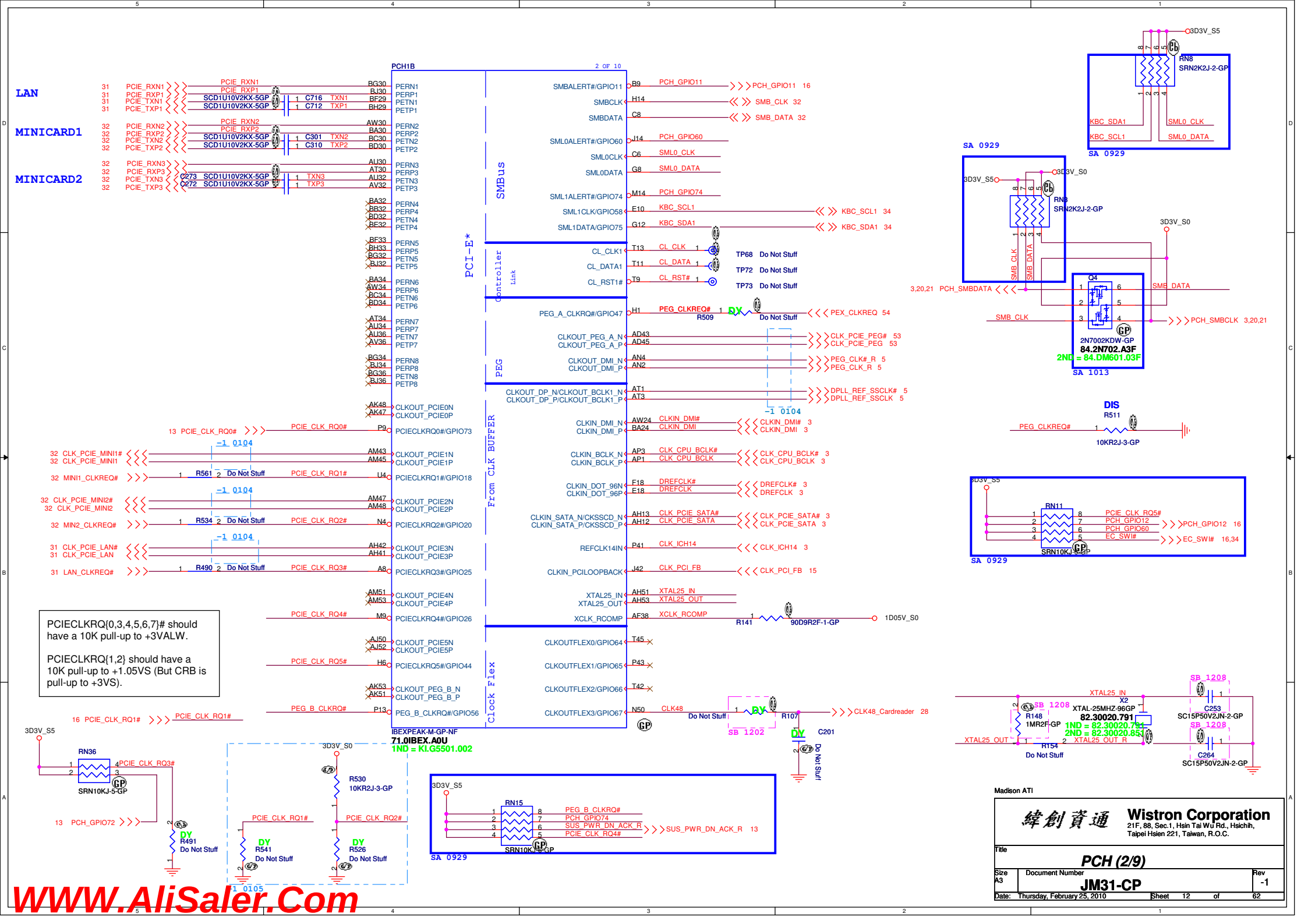
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SA 0929
SA 1013
DIS
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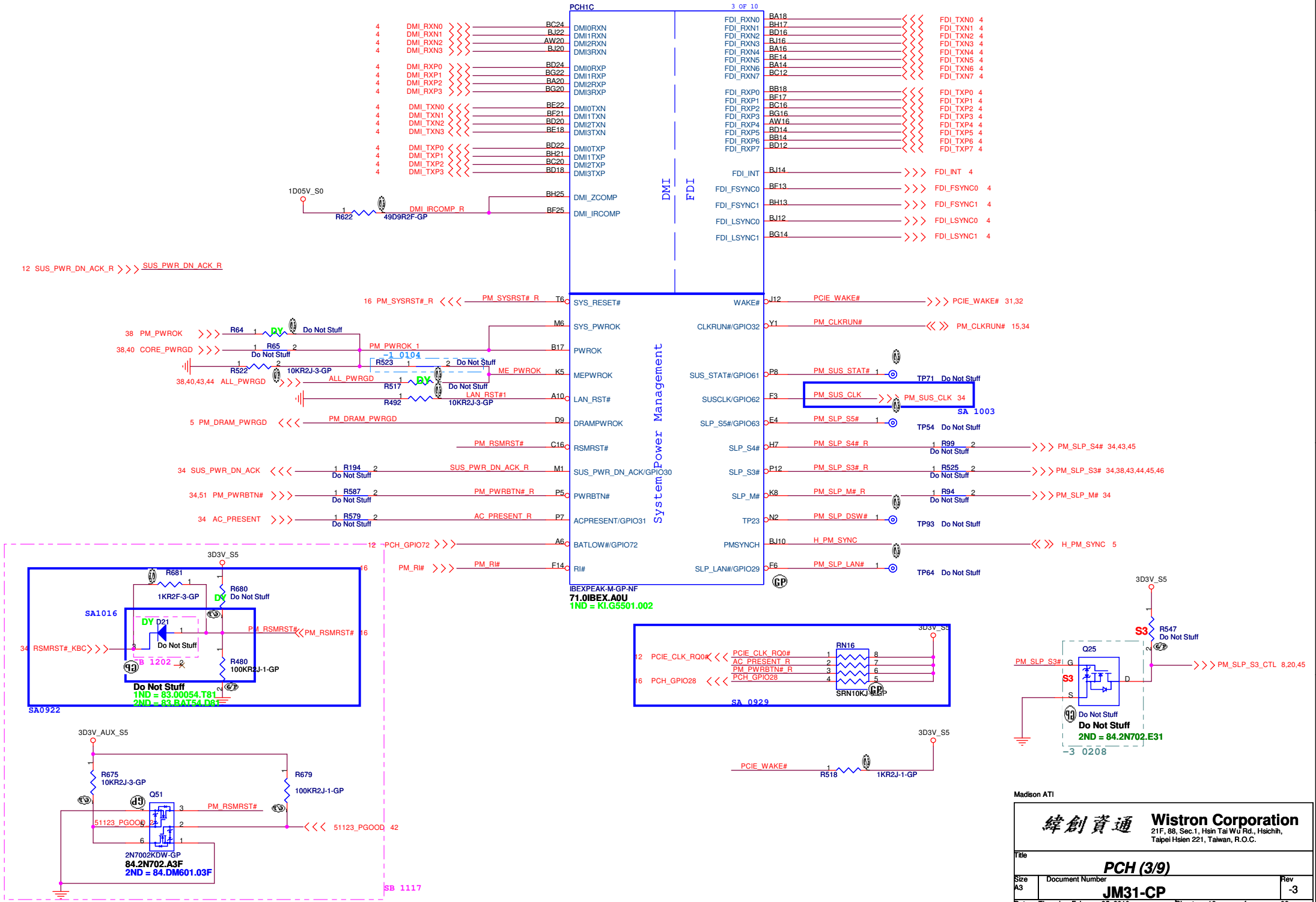
PCH1C
3 OF 10
DMI
FDI
System Power Management
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#/GPIO29
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
1D05V_S0
R622
49D9R2F-GP
DMI_IRCOMP_R
12 SUS_PWR_DN_ACK_R
16 PM_SYSRST#_R
38 PM_PWROK
38,40 CORE_PWRGD
38,40,43,44 ALL_PWRGD
5 PM_DRAM_PWRGD
34 SUS_PWR_DN_ACK
34,51 PM_PWRBTN#
34 AC_PRESENT
12 PCH_GPIO72
PM_RI#
R64
R65
R522
R523
R517
R492
10KR2J-3-GP
ME_PWROK
LAN_RST#1
R194
R587
R579
R681
1KR2F-3-GP
R680
SA1016
D21
R480
100KR2J-1-GP
SB 1202
SA0922
1ND = 83.00054.T81
2ND = 83.BAT54.D81
34 RSMRST#_KBC
3D3V_AUX_S5
R675
10KR2J-3-GP
R679
100KR2J-1-GP
Q51
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
SB 1117
51123_PGOOD
42
PCIE_CLK_RQ0#
16 PCH_GPIO28
RN16
SRN10KJ-GP
SA 0929
PCIE_WAKE#
R518
1KR2J-1-GP
PM_SUS_STAT#
TP71 Do Not Stuff
PM_SUS_CLK
SA 1003
PM_SUS_S5#
TP54 Do Not Stuff
PM_SLP_S4#
R99
PM_SLP_S3#
R525
PM_SLP_M#
R94
PM_SLP_DSW#
TP93 Do Not Stuff
H_PM_SYNC
PM_SLP_LAN#
TP64 Do Not Stuff
PCIE_WAKE#
PCIE_CLK_RQ0#
AC_PRESENT_R
PM_PWRBTN#_R
PCH_GPIO28
FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
S3
R547
Q25
PM_SLP_S3_CTL 8,20,45
2ND = 84.2N702.E31
-3 0208
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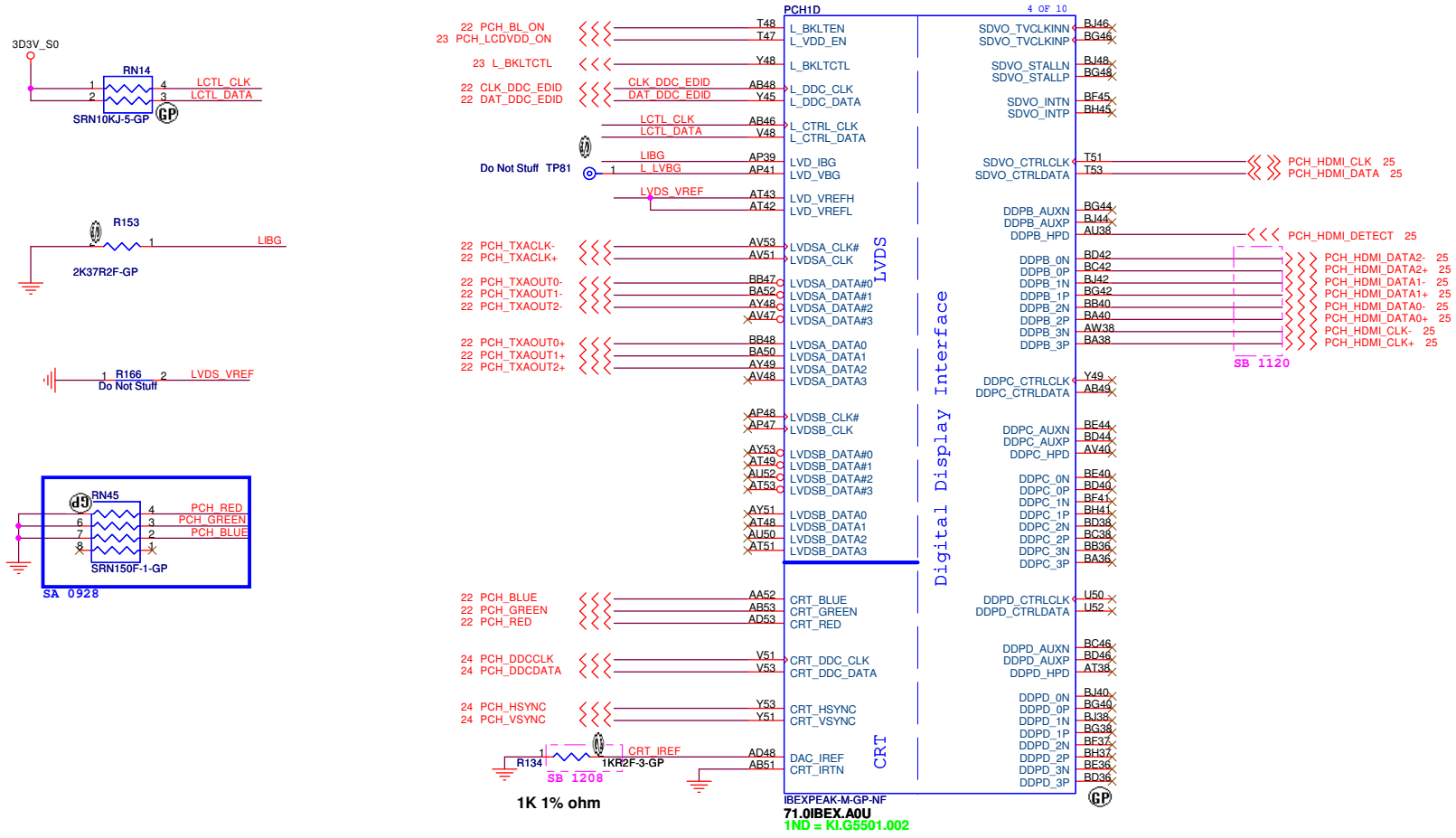

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These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	EXT USB1
1	USB1(on board)
2	EXT USB2
3	MINICARD1
4	WECAM
5	SIM Card
6	NC
7	NC
8	NC
9	NC
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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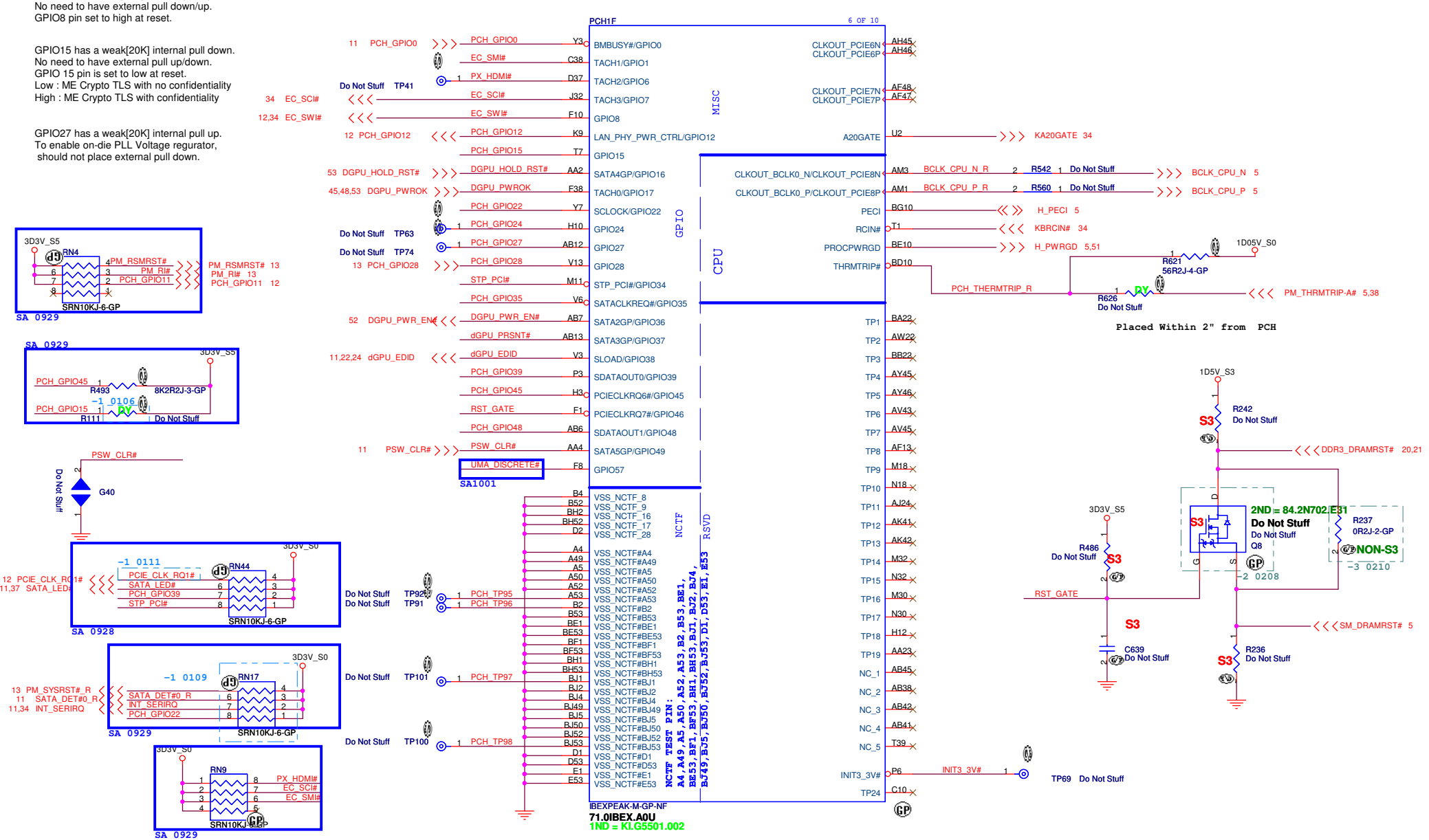
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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Title: **PCH (6/9)**

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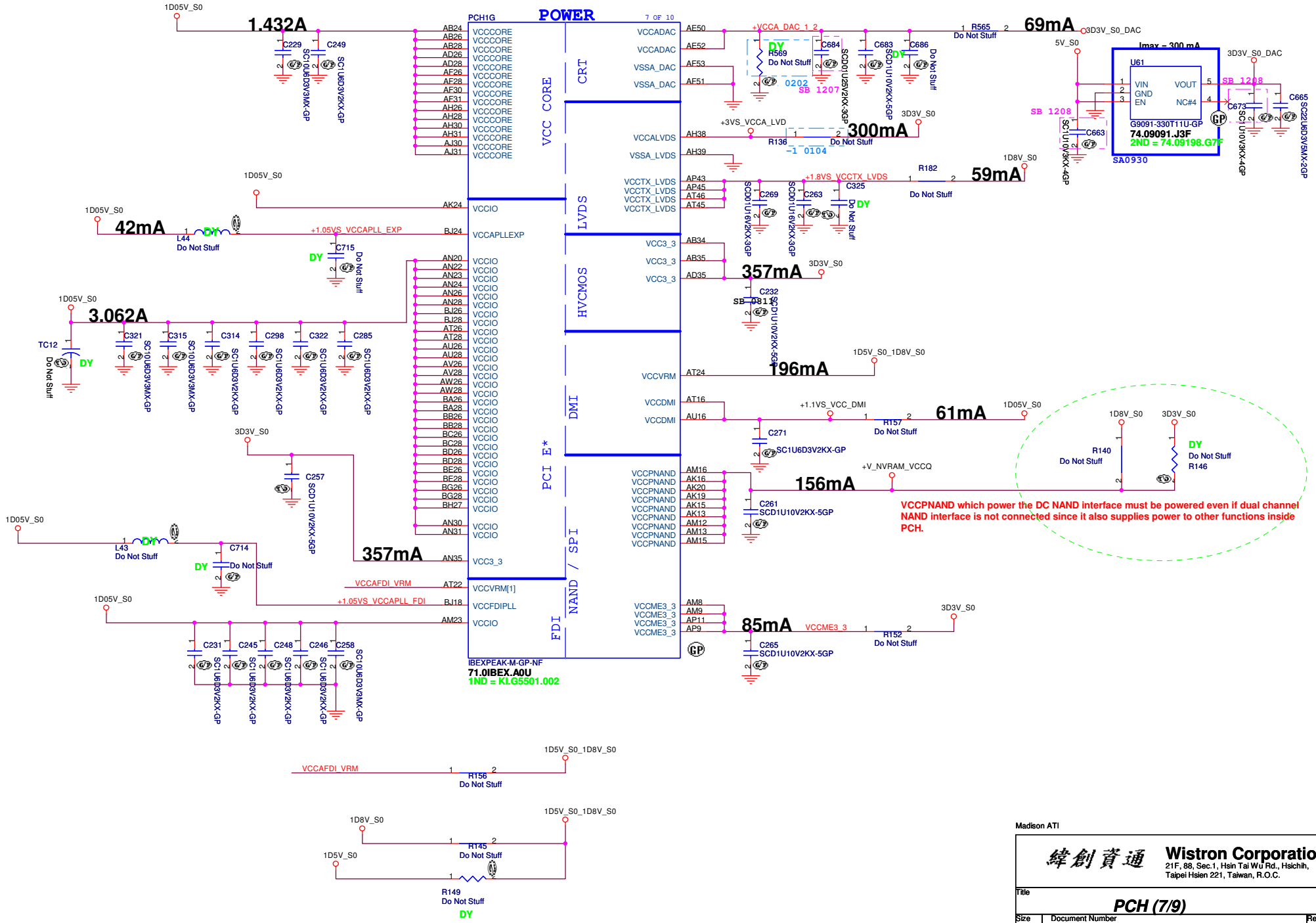

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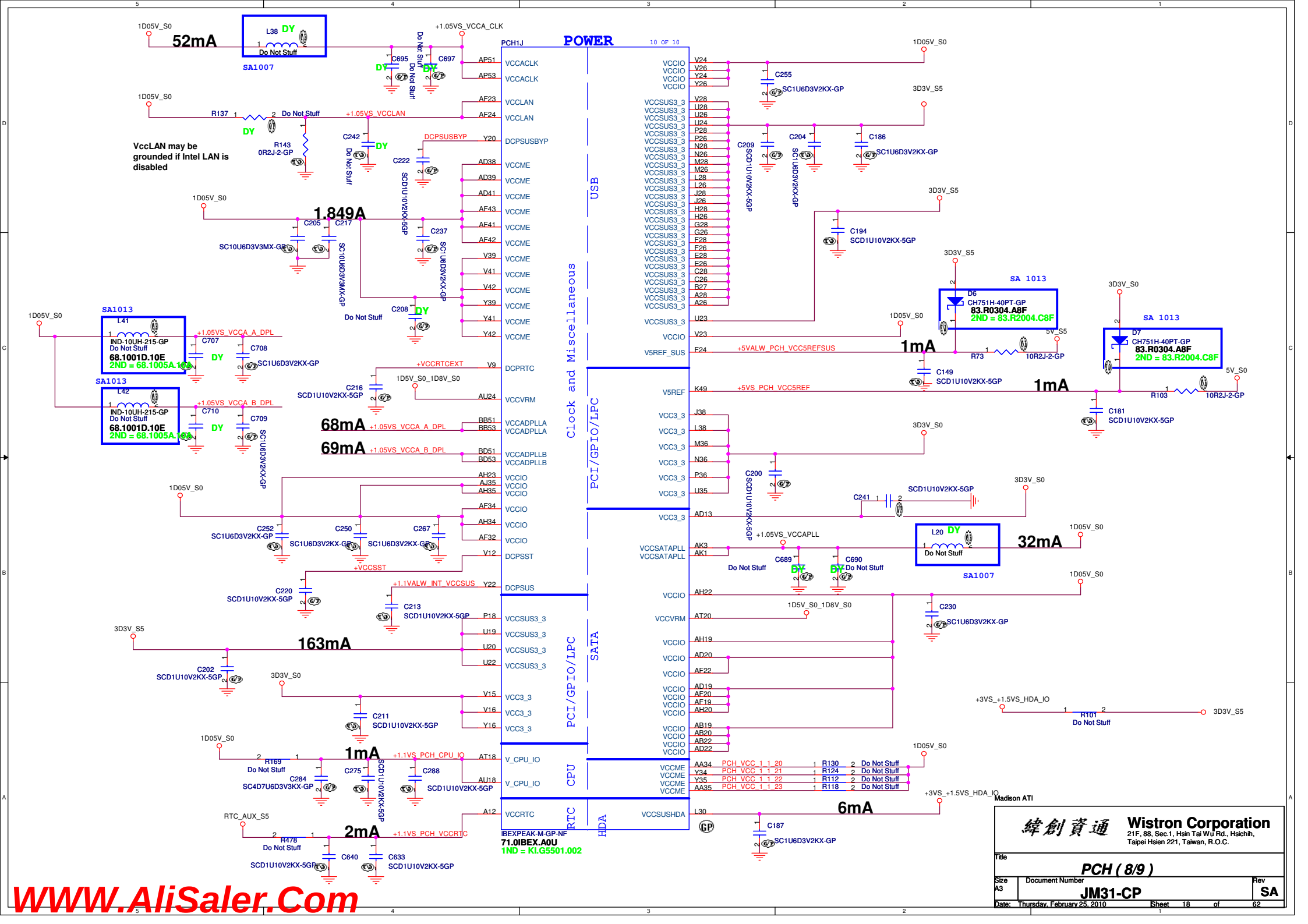
POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
VccLAN may be grounded if Intel LAN is disabled
SA1007
SA1013
DY
Do Not Stuff
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
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PCH (8/9)
JM31-CP
SA
Thursday, February 25, 2010
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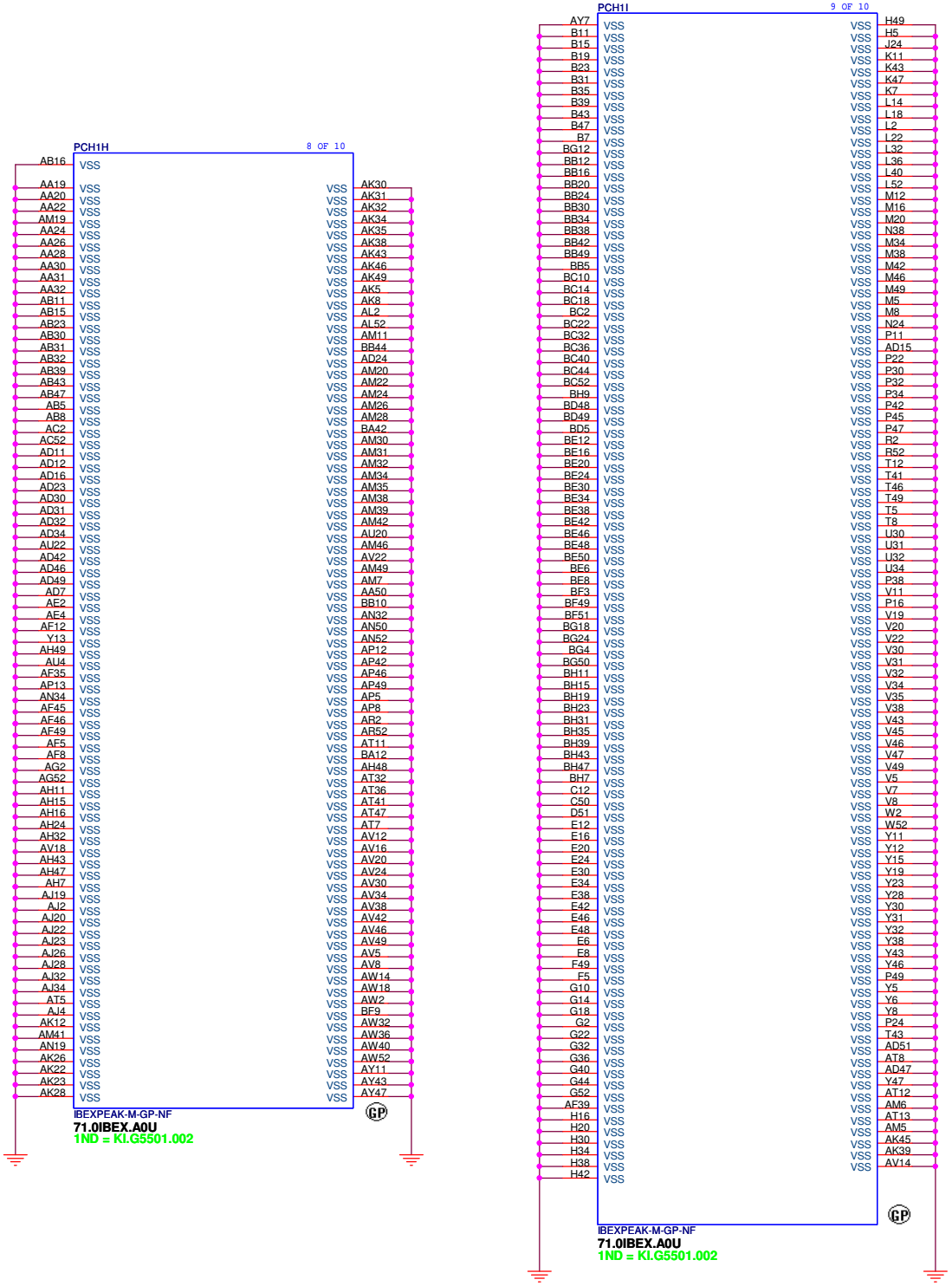

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***PCH (9/9)***	
Size A3	Document Number **J\M31-CP**	Rev **SA**
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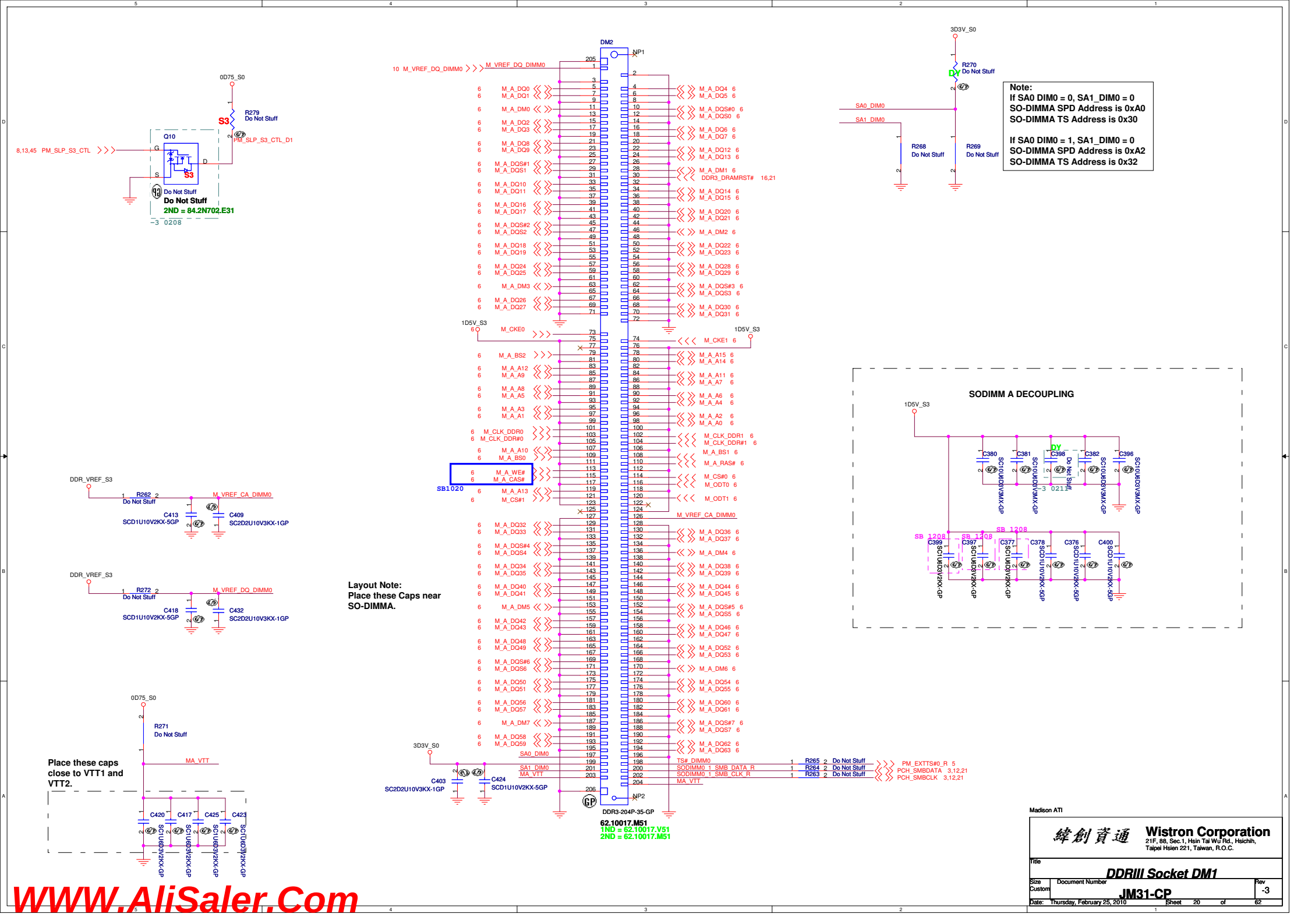

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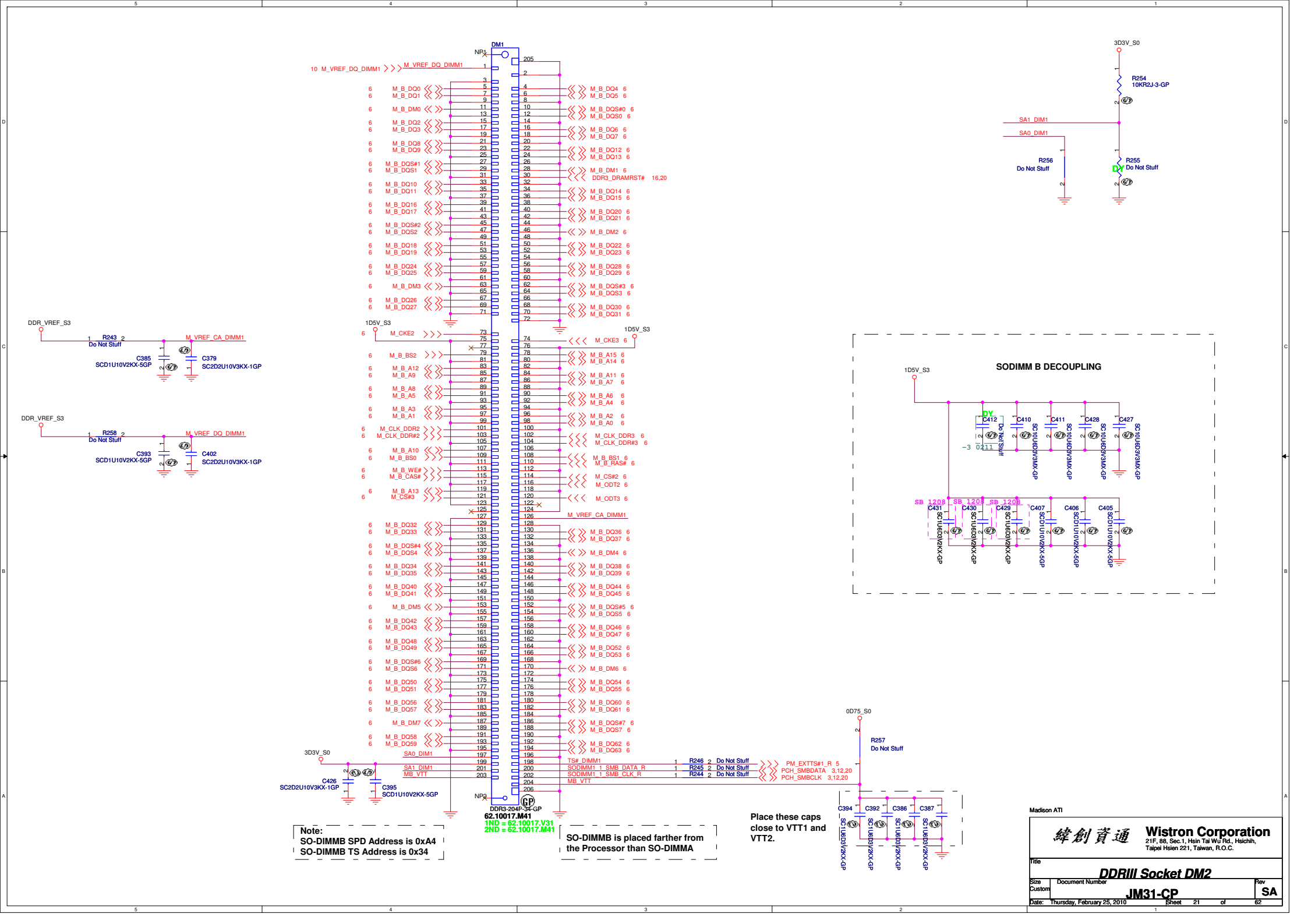
DM1
NP1
NP2
DDR3-204P-34-GP
62.10017.M41
1ND = 62.10017.V31
2ND = 62.10017.M41
M_VREF_DQ_DIMM1
M_VREF_CA_DIMM1
M_CKE2
M_CKE3
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
M_B_BS2
M_B_BS1
M_B_RAS#
M_B_WE#
M_B_CAS#
M_CS#2
M_CS#3
M_ODT2
M_ODT3
DDR3_DRAMRST#
TS#_DIMM1
SODIMM1_1_SMB_DATA_R
SODIMM1_1_SMB_CLK_R
PM_EXTTS#1_R
PCH_SMBDATA
PCH_SMBCLK
SA0_DIM1
SA1_DIM1
MB_VTT
DDR_VREF_S3
1D5V_S3
3D3V_S0
0D75_S0
R243 Do Not Stuff
R258 Do Not Stuff
R246 Do Not Stuff
R245 Do Not Stuff
R244 Do Not Stuff
R254 10KR2J-3-GP
R256 Do Not Stuff
R255 Do Not Stuff
R257 Do Not Stuff
C385 SCD1U10V2KX-5GP
C379 SC2D2U10V3KX-1GP
C393 SCD1U10V2KX-5GP
C402 SC2D2U10V3KX-1GP
C426 SC2D2U10V3KX-1GP
C395 SCD1U10V2KX-5GP
SODIMM B DECOUPLING
C412 DY Do Not Stuff
C410 SC10U6D3V3MX-GP
C411 SC10U6D3V3MX-GP
C428 SC10U6D3V3MX-GP
C427 SC10U6D3V3MX-GP
C431 SC10U6D3V2KX-GP
C430 SC10U6D3V2KX-GP
C429 SC10U6D3V2KX-GP
C407 SC1U10V2KX-5GP
C406 SC1U10V2KX-5GP
C405 SC1U10V2KX-5GP
C394 SC10U6D3V2KX-GP
C392 SC10U6D3V2KX-GP
C386 SC10U6D3V2KX-GP
C387 SC10U6D3V2KX-GP
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
Place these caps close to VTT1 and VTT2.
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Title
DDRIII Socket DM2
Size Custom
Document Number
JM31-CP
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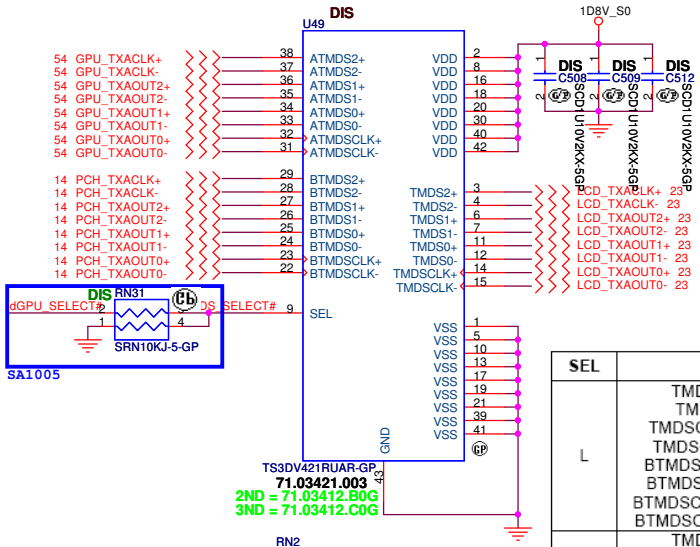
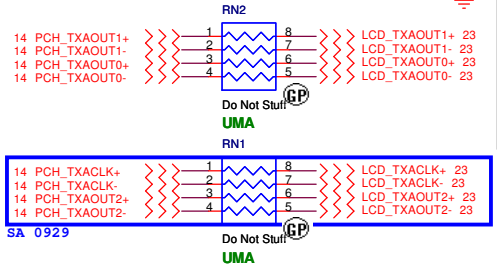


FUNCTION TABLE

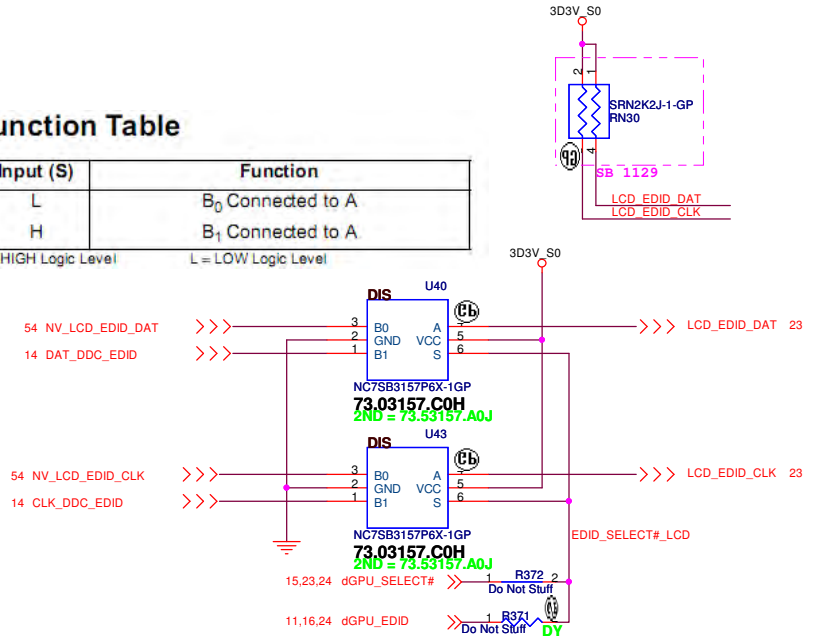
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

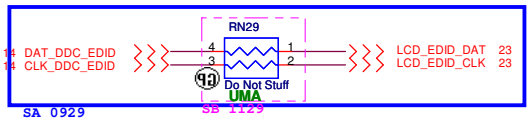
H = HIGH Logic Level L = LOW Logic Level

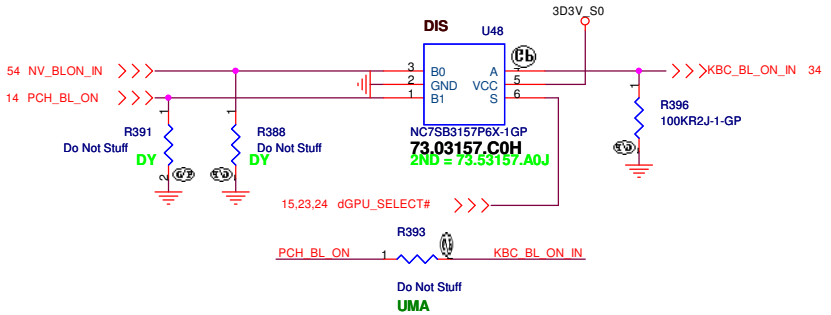


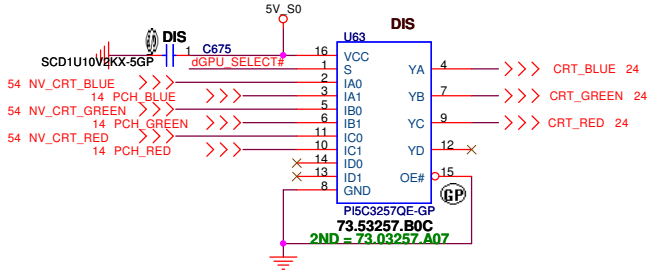
Function Table

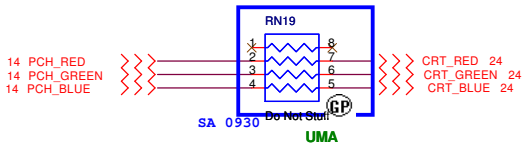
Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level









$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: PX SWITCH

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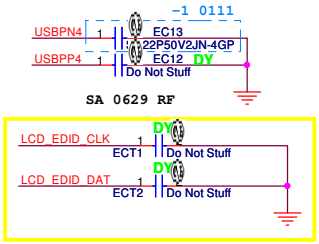
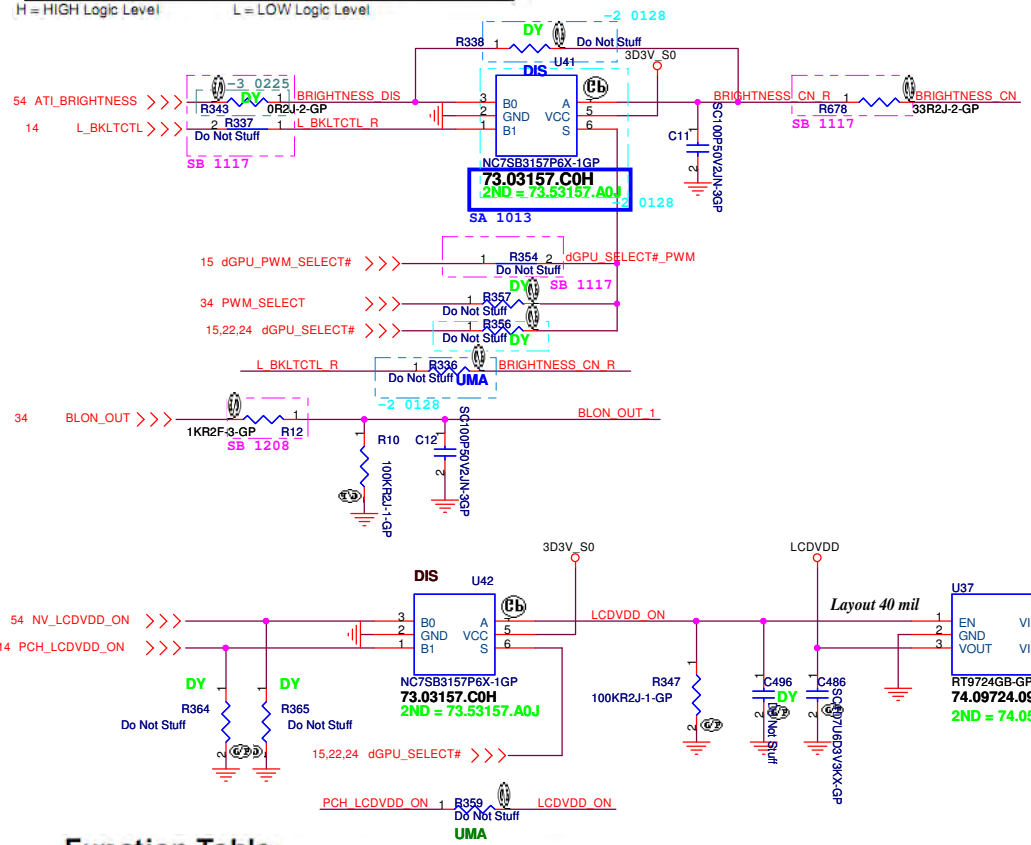
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

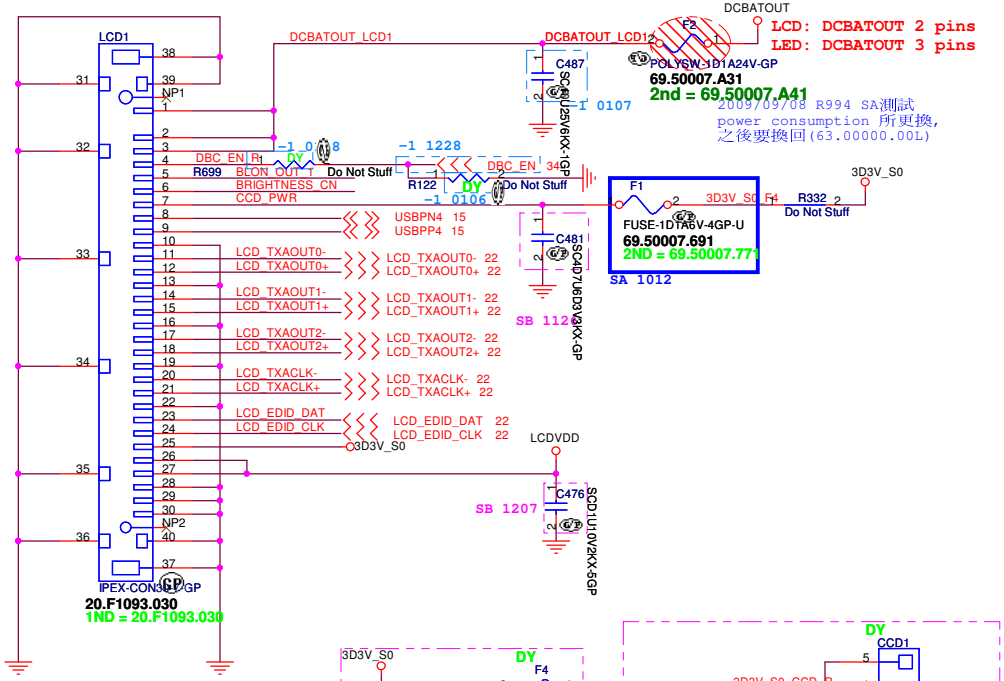
H = HIGH Logic Level L = LOW Logic Level

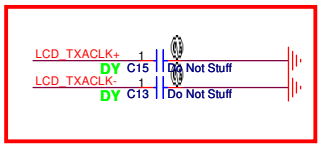


Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level





modify by RF

Reserve direct connector to KBC

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Title: **LCD CONN**

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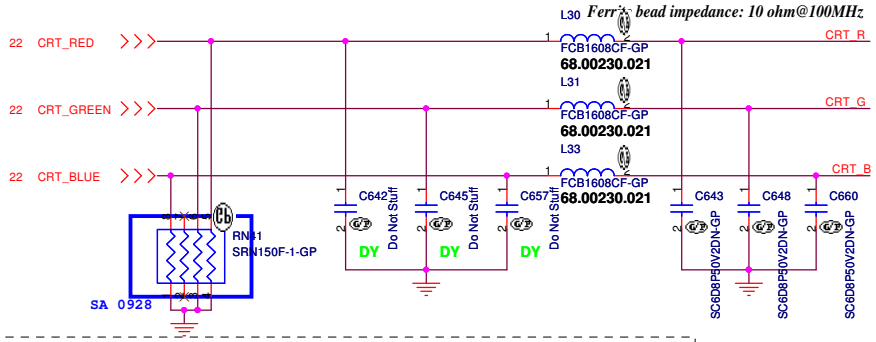
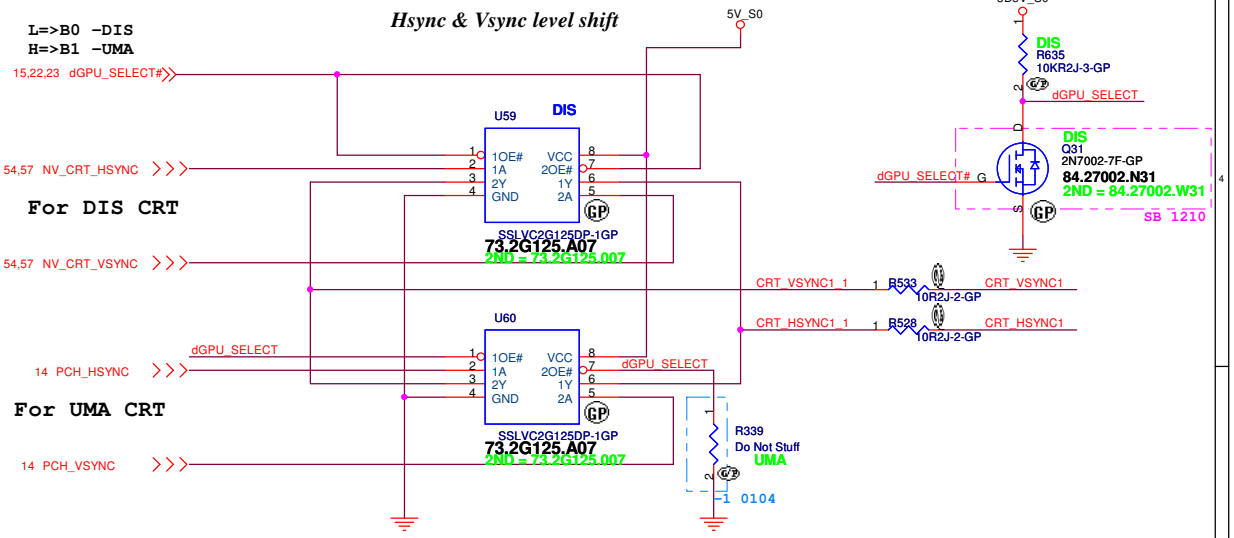
Layout Note:
Place these resistors close to the CRT-out connector

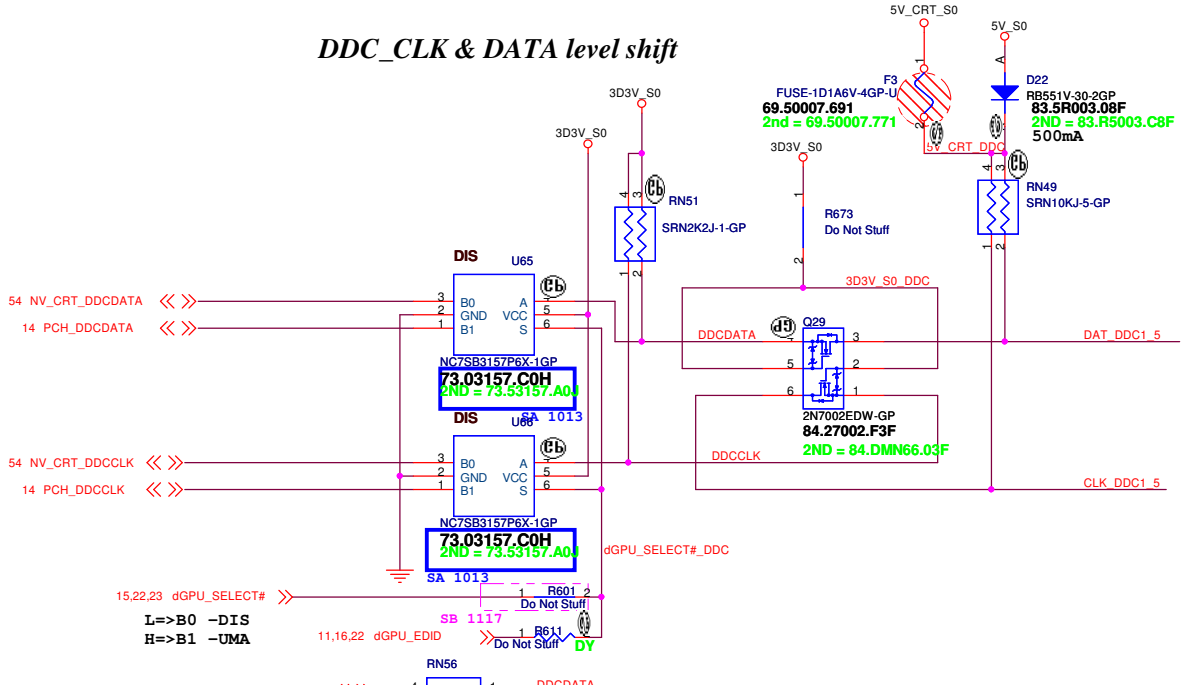


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

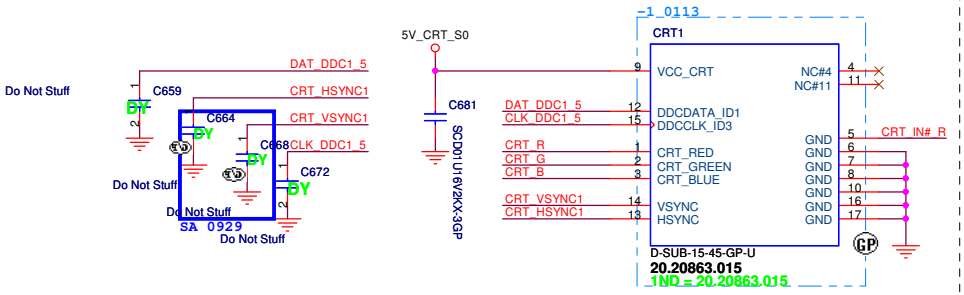
Hsync & Vsync level shift

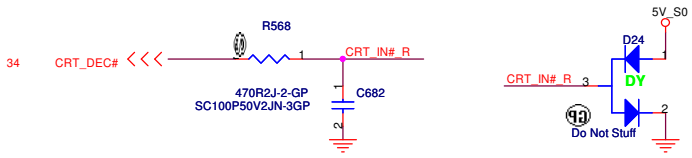


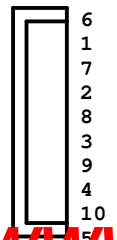
DDC_CLK & DATA level shift



CRT I/F & CONNECTOR







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Title: **CRT CONN**

Size	Document Number	Rev
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Close HDMI1

SB 1209

HDMI1
SKT-HDMI23-1-GP
22.10296.181
1ND = 22.10296.181
2ND = 22.10296.211
-1 0111

HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP83 Do Not Stuff
TDMS_A_CLK
TDMS_A_DAT
5V_HDMI
-2 0127
HDMI_A_HPD_CN
R637 10KR2J-3-GP
-1 0105
R629 100KR2J-1-GP
NV_HDMI_DETECT

5V_S0
D26
HDMI_A_HPD_CN
DY
Do Not Stuff

3D3V_S0
RN57
Do Not Stuff
UMA
Do Not Stuff
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA

RN61
SRN2K2J-1-GP
66.22236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D25
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.G11
EC84 DY
EC85 DY
Do Not Stuff

5V_HDMI
-3 0210
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
R703 DY Do Not Stuff
-2 0127
-3 0210

3D3V_VGA
RN25
Do Not Stuff
54 NV_HDMI_CLK
54 NV_HDMI_DATA
PCH_HDMI_DATA
PCH_HDMI_CLK
RN71
Do Not Stuff
UMA
-1 0105
U20 DY
1OE# 1A 1B GND VCC 2OE# 2B 2A
TDMS_A_CLK
TDMS_A_DAT
5V_S0
Do Not Stuff
Do Not Stuff
2ND = 73.03306.D0B

SA1001
3D3V_HDMI
SB 1125
Q7 UMA
54 NV_HDMI_CLK
54 NV_HDMI_DATA
TDMS_A_CLK
TDMS_A_DAT
Do Not Stuff
Do Not Stuff
2ND = 84.DMN66.03F

54 NV_HDMI_DATA0-
54 NV_HDMI_DATA0+
54 NV_HDMI_DATA1-
54 NV_HDMI_DATA1+
54 NV_HDMI_DATA2-
54 NV_HDMI_DATA2+
54 NV_HDMI_CLK-
54 NV_HDMI_CLK+
From VGA on board
DIS C342 SCD1U10V2KX-5GP HDMI_TX0-
DIS C340 SCD1U10V2KX-5GP HDMI_TX0+
DIS C328 SCD1U10V2KX-5GP HDMI_TX1-
DIS C324 SCD1U10V2KX-5GP HDMI_TX1+
DIS C317 SCD1U10V2KX-5GP HDMI_TX2-
DIS C313 SCD1U10V2KX-5GP HDMI_TX2+
DIS C335 SCD1U10V2KX-5GP HDMI_TXC-
DIS C332 SCD1U10V2KX-5GP HDMI_TXC+
SB 1207

3D3V_S0
C717 DY
C713 DY
C705 DY
C711 DY
Do Not Stuff
SB 1130
R634 DY
R633 DY
NC#35
NC#34

SA 1002
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
From PCH

U67
VCC GND
IN_D1- IN_D1+
IN_D2- IN_D2+
IN_D3- IN_D3+
IN_D4- IN_D4+
OUT_D1- OUT_D1+
OUT_D2- OUT_D2+
OUT_D3- OUT_D3+
OUT_D4- OUT_D4+
PC0 PC1
REXT RT_EN# OE# DDC_EN
SDA SCL HPD
HPD_SINK SDA_SINK SCL_SINK
Do Not Stuff
DY
Do Not Stuff

SA 1002
HDMI_TX0- HDMI_TX0+
HDMI_TXC- HDMI_TXC+
HDMI_TX1- HDMI_TX1+
HDMI_TX2- HDMI_TX2+

Recommended Equalization: [PC1,PC0]=01, 4dB
SB 1130
3D3V_S0
R607 DY Do Not Stuff PC0
R606 DY Do Not Stuff PC1
R605 DY Do Not Stuff
REXT_HDMI
PS8101_RT_EN#
OE# PS8101
DDC_EN_PS8101

PCH_HDMI_DETECT 14
HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
RN23
SRN0J-6-GP
DIS
SB 1119
NV_HDMI_DATA 54
NV_HDMI_CLK 54
R603 Do Not Stuff DY

HDMI_TX0- HDMI_TX0+ R627 R625
HDMI_TX1- HDMI_TX1+ R619 R617
HDMI_TX2- HDMI_TX2+ R615 R613
HDMI_TXC- HDMI_TXC+ R624 R620
562R2F-GP
DIS 64.49905.6DL/ UMA:64.56205.6DL
SB 1202

SB 1125
3D3V_S0 3D3V_VGA
R180 0R2J-2-GP
R179 Do Not Stuff DY
3D3V_HDMI
SB 1210
Q22 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
G NV_HDMI_DETECT
34,54 HPD1
PCH_HDMI_DETECT
R178 UMA Do Not Stuff
SB 1125
R524 10KR2J-3-GP
-1 0105

3D3V_S0
R628 Do Not Stuff DY
OE# PS8101
Q36 Do Not Stuff
Do Not Stuff
2ND = 84.27002.W31
DY
HDMI_A_HPD_CN
R631 DY Do Not Stuff
SB 1210
SB 1207

Q5 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
3D3V_S0
R201 DY Do Not Stuff
SA 0929

REXT_HDMI
PS8101_RT_EN#
R604 Do Not Stuff DY
R602 Do Not Stuff DY
SB 1202

3D3V_S0
SB 1202
R632 Do Not Stuff DY
DDC_EN_PS8101

PCH_HDMI_CLK- PCH_HDMI_CLK+ UMA C339 C334 Do Not Stuff HDMI_TXC-
PCH_HDMI_DATA0- PCH_HDMI_DATA0+ UMA C344 C341 Do Not Stuff HDMI_TX0-
PCH_HDMI_DATA1- PCH_HDMI_DATA1+ UMA C327 C323 Do Not Stuff HDMI_TX1-
PCH_HDMI_DATA2- PCH_HDMI_DATA2+ UMA C316 C312 Do Not Stuff HDMI_TX2-
SA1001
SB 1207

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Title: HDMI CONNECTOR
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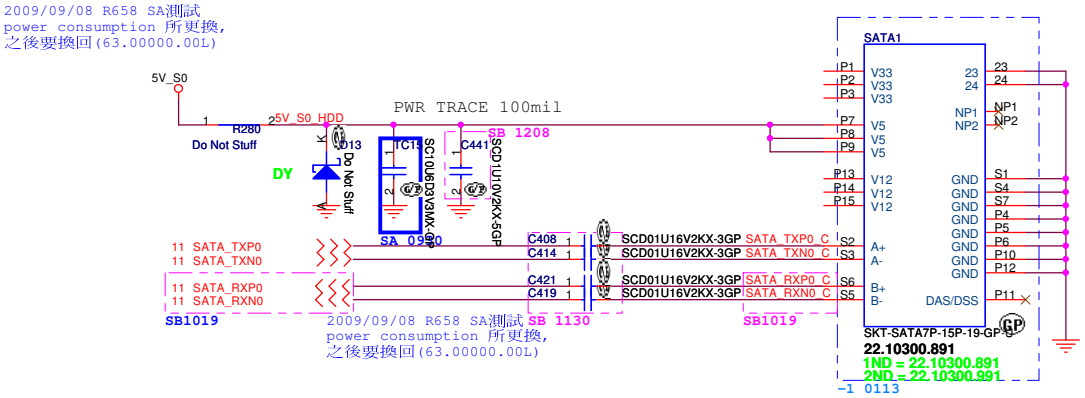
SATA Connector



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Title: HDD CONN

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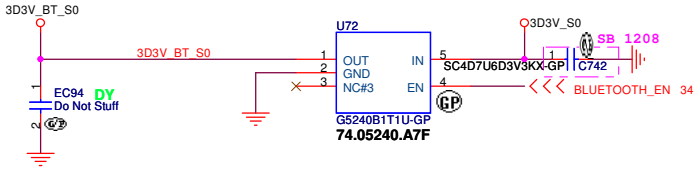
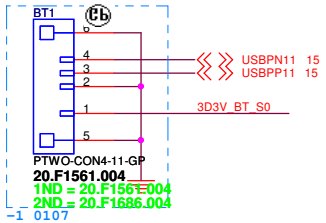
BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



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Title: ***BLUETOOTH***		
Size: A3	Document Number: **JM31-CP**	Rev: -1
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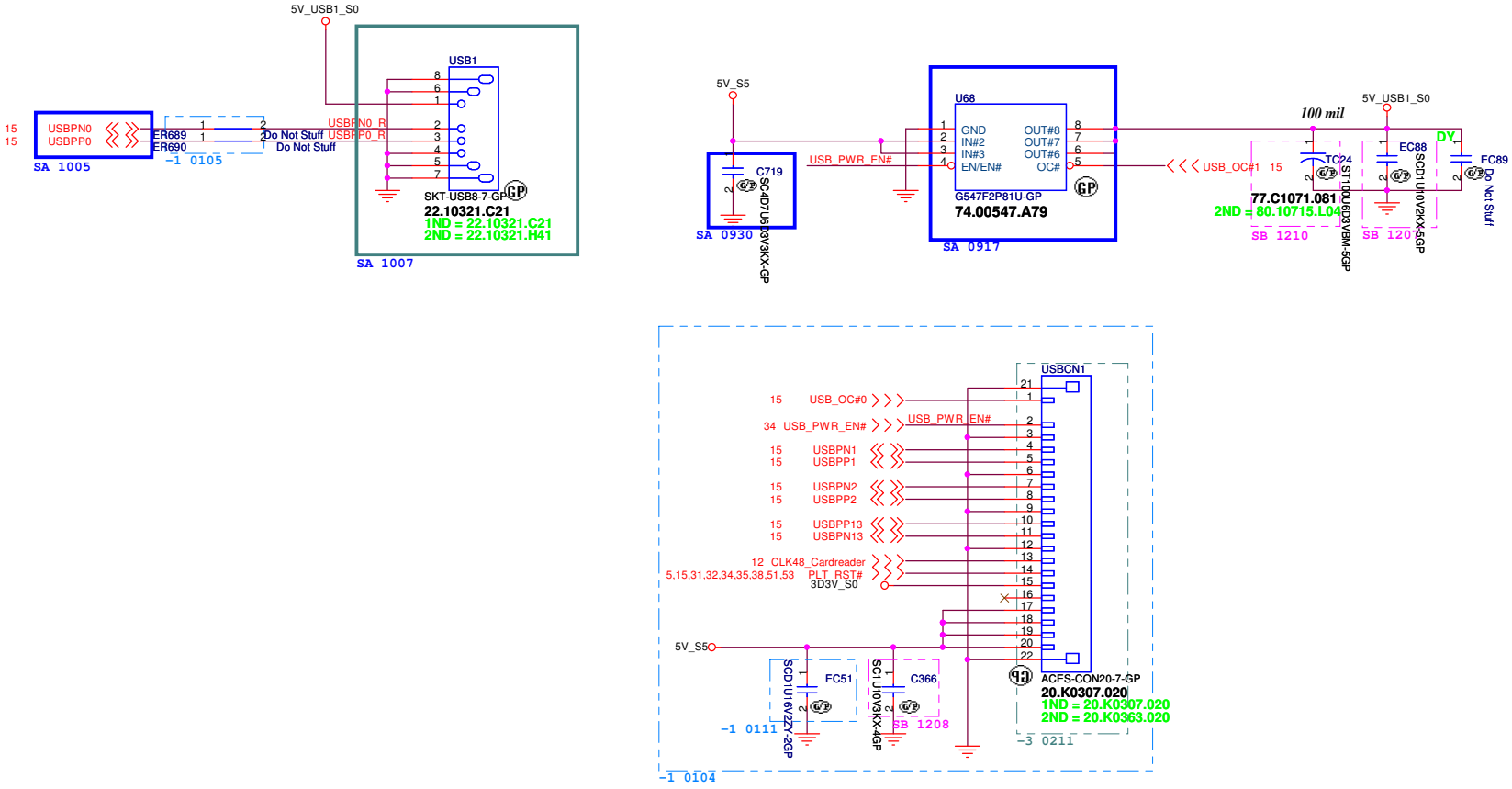

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Title		
USB CONN		
Size: A3	Document Number: JM31-CP	Rev: -3
Date: Thursday, February 25, 2010	Sheet 28 of 62	

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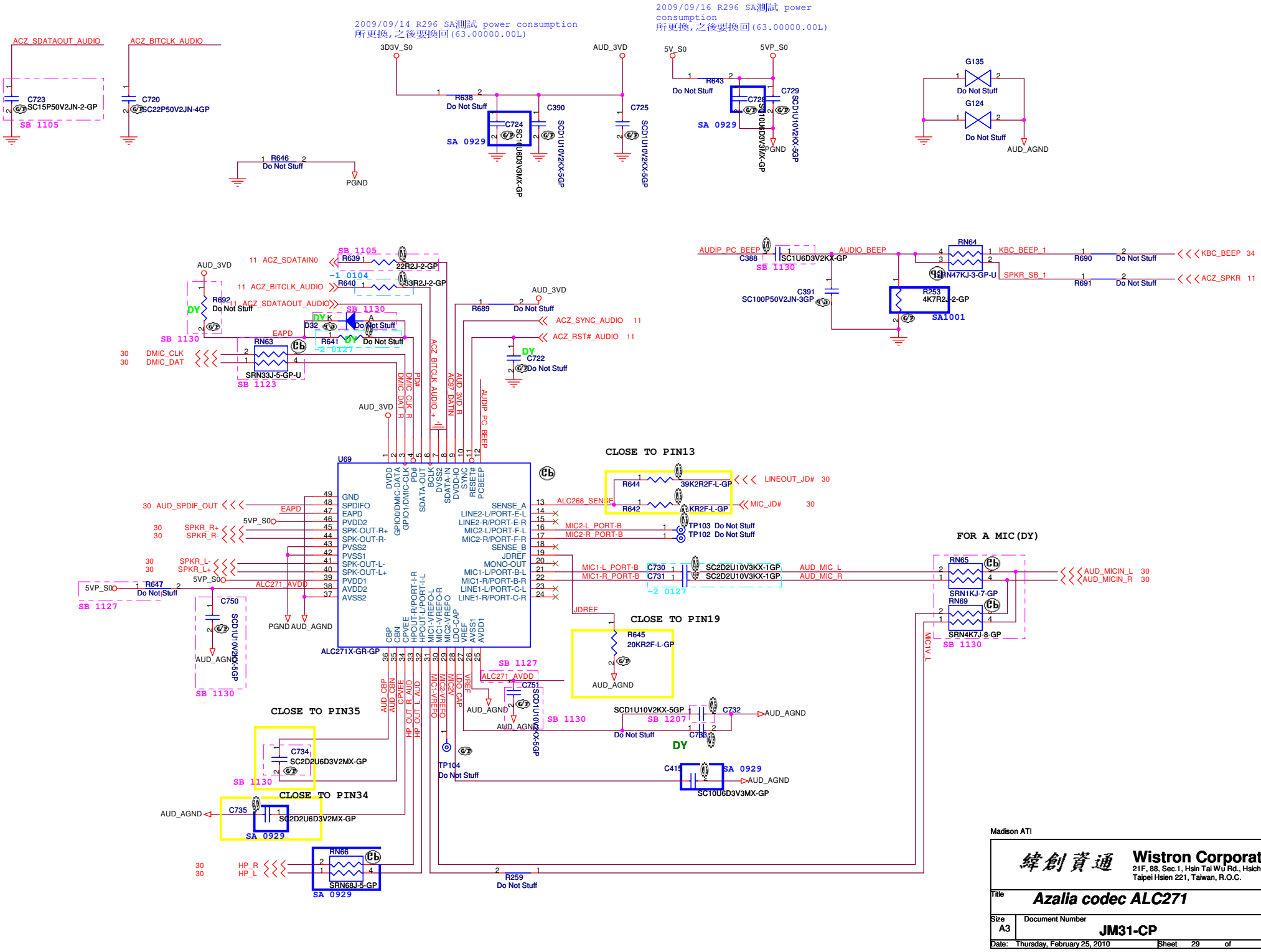

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Azalia codec ALC271	
Size A3	Document Number JM31-CP	Rev SB
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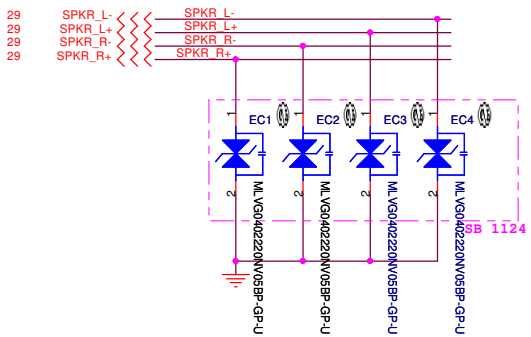
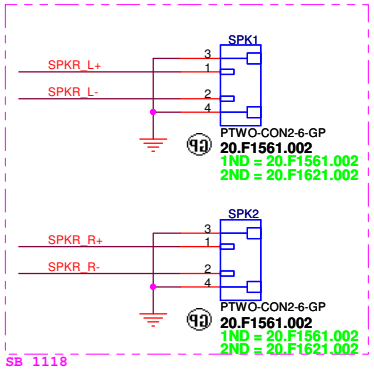
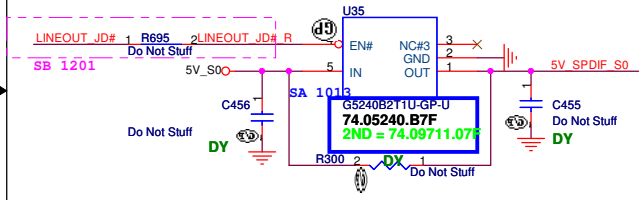
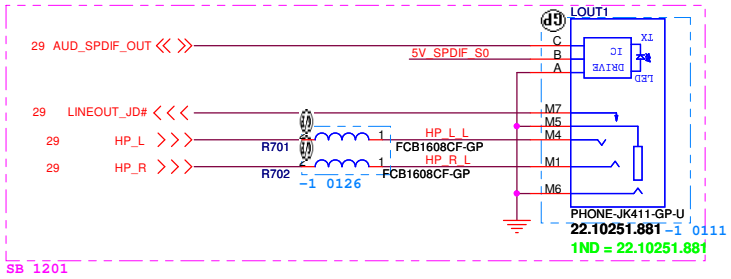
Internal Speaker

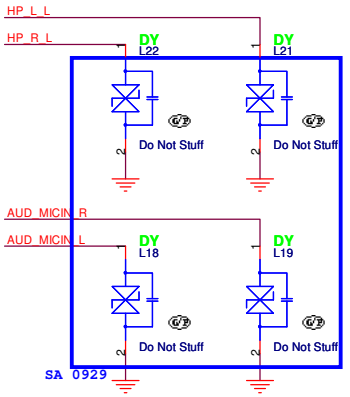




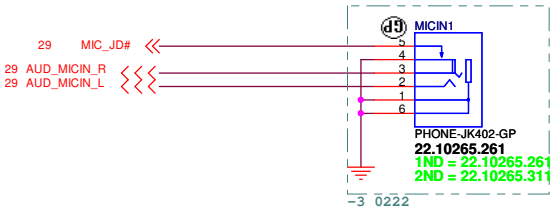
LINE OUT

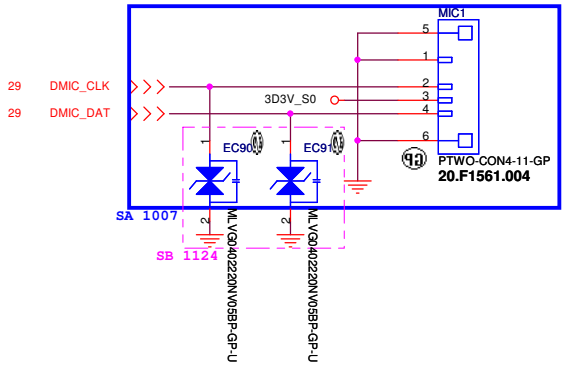






MIC IN





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Title	AUDIO jack	
Size A3	Document Number JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 30 of 62	

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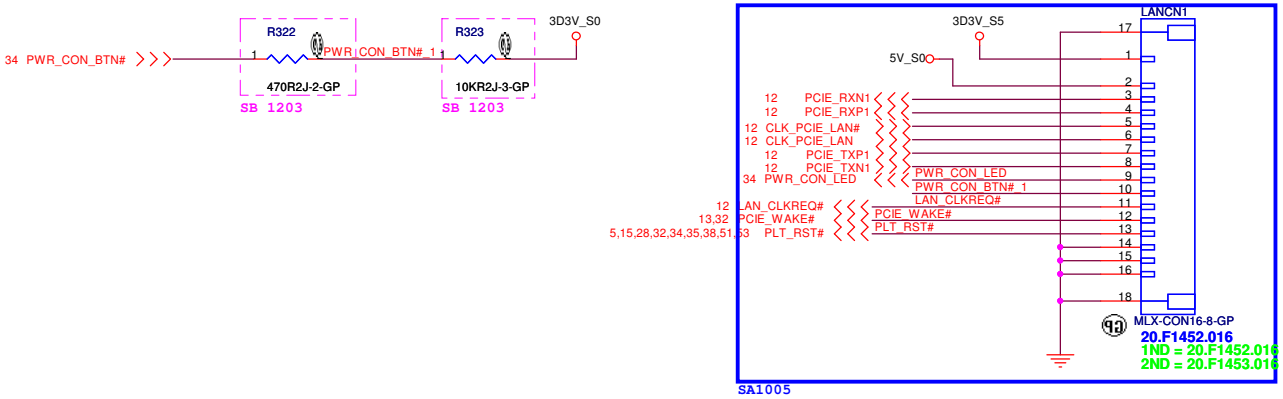

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Title		
LAN CONN		
Size: A3	Document Number: **JM31-CP**	Rev: SB
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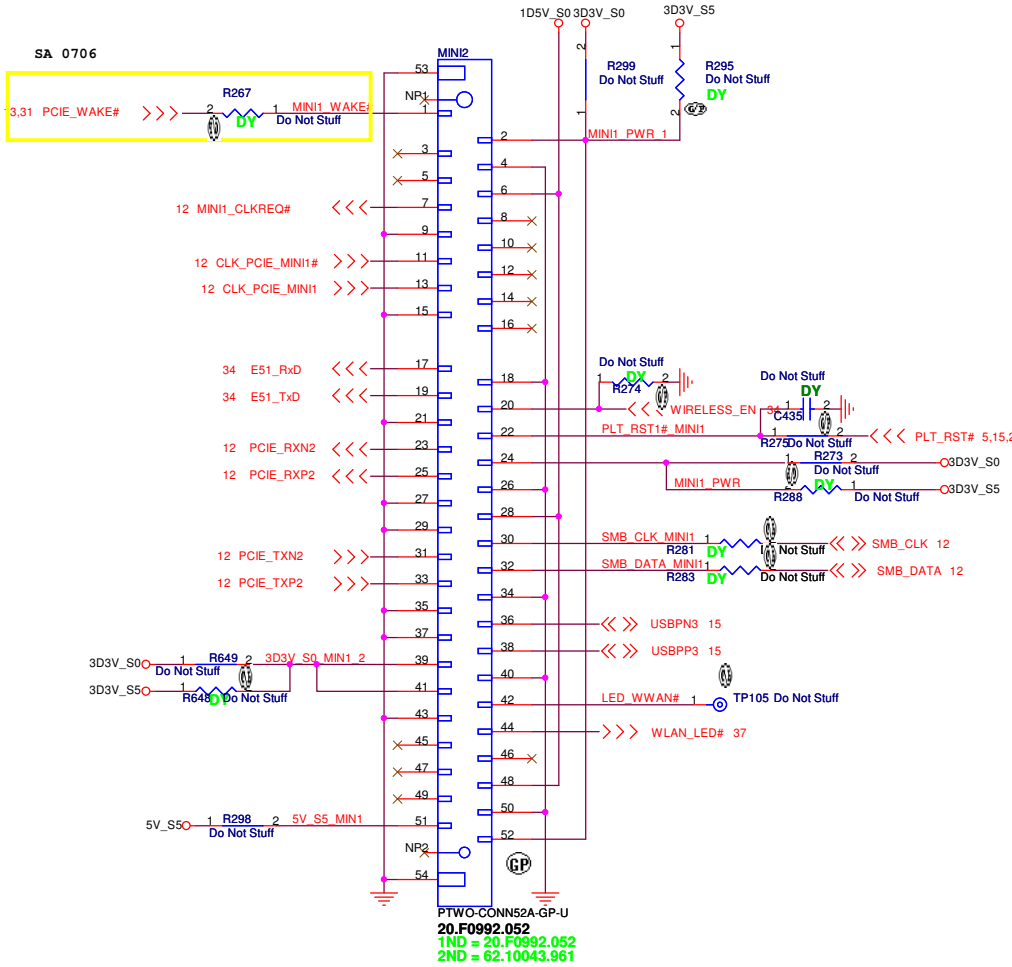
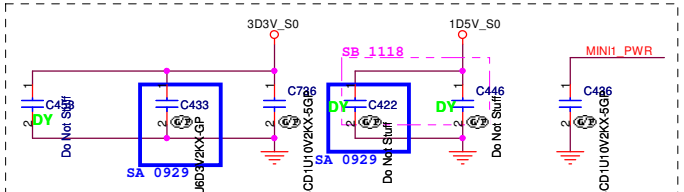
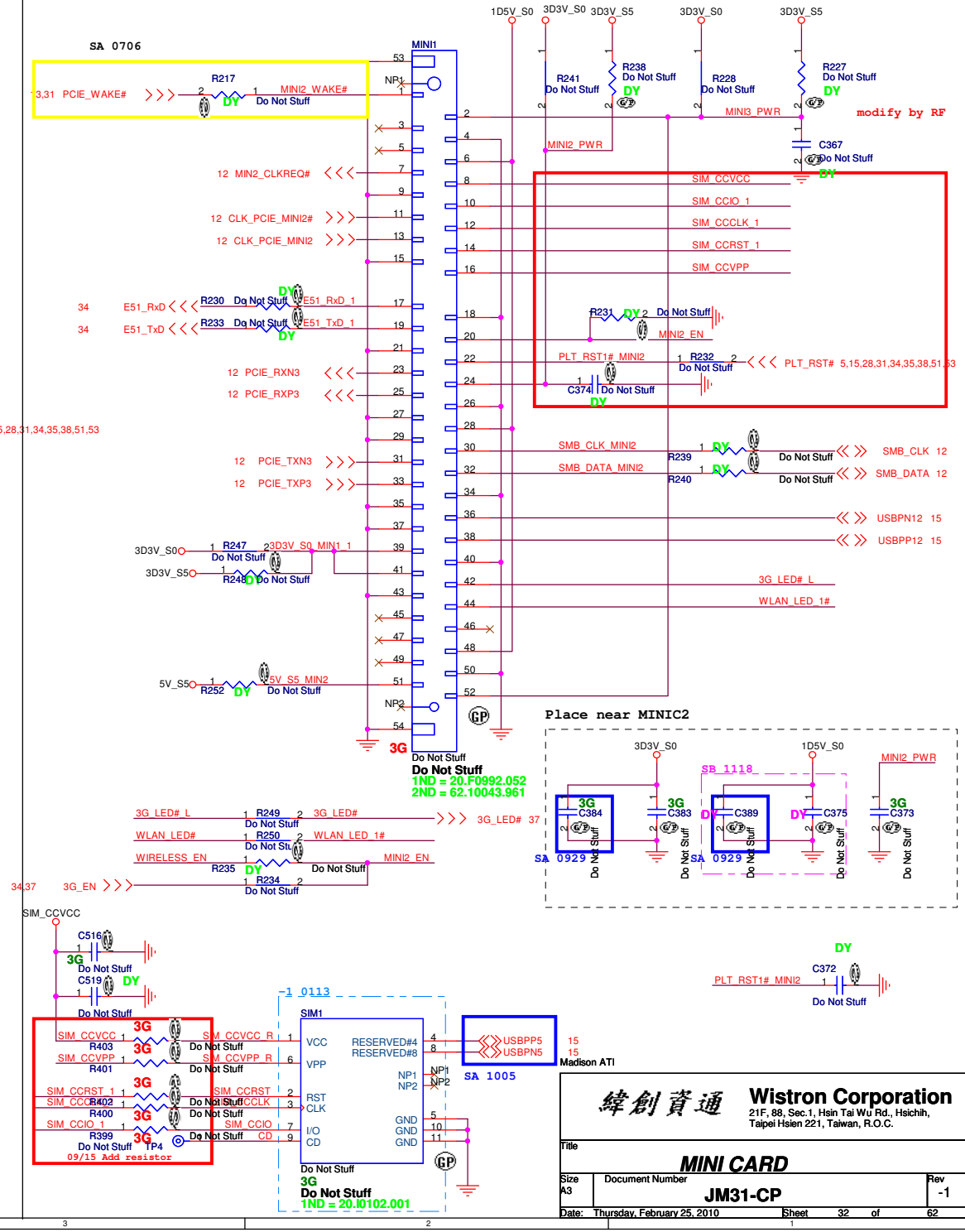
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector(Robson2 and 3G)



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size	Document Number	Rev
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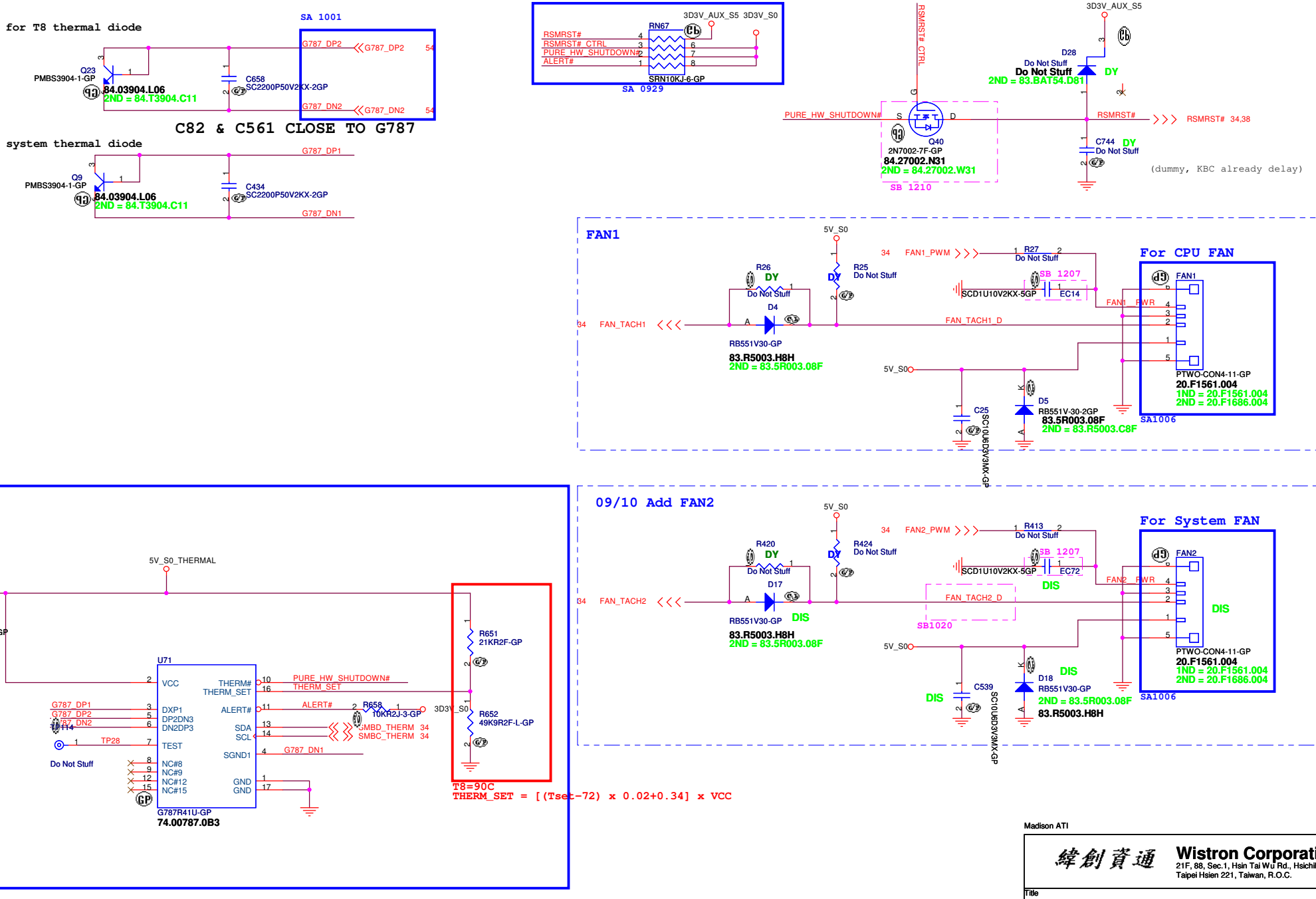

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Title: ***Thermal/Fan Connector***

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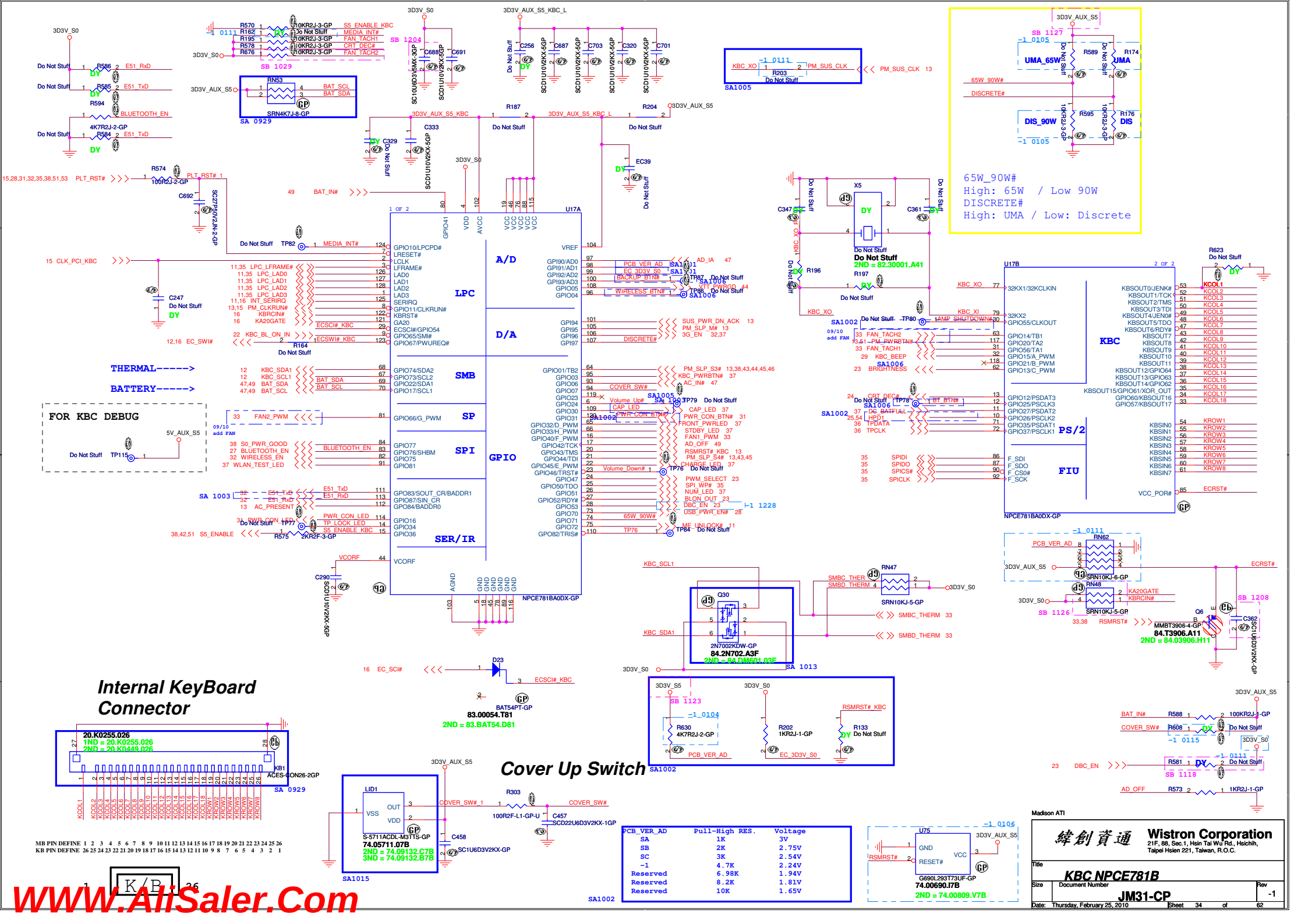
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
U17A
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U17B
KBC
PS/2
FIU
NPCE781BA0DX-GP
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
Cover Up Switch
20.K0255.026
1ND = 20.K0255.026
2ND = 20.K0449.026
ACES-CON26-2GP
S-5711ACDL-M3TS-GP
74.05711.07B
2ND = 74.09132.C7B
3ND = 74.09132.B7B
2N7002KDW-GP
84.2N702.A3F
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
MMBT3906-4-GP
84.T3906.A11
2ND = 84.03906.H11
G690L293T3UF-GP
74.00690.I7B
2ND = 74.00809.V7B
PCB_VER_AD | Pull-High RES. | Voltage
SA | 1K | 3V
SB | 2K | 2.75V
SC | 3K | 2.54V
-1 | 4.7K | 2.24V
Reserved | 6.98K | 1.94V
Reserved | 8.2K | 1.81V
Reserved | 10K | 1.65V
MB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
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Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
JM31-CP
Thursday, February 25, 2010
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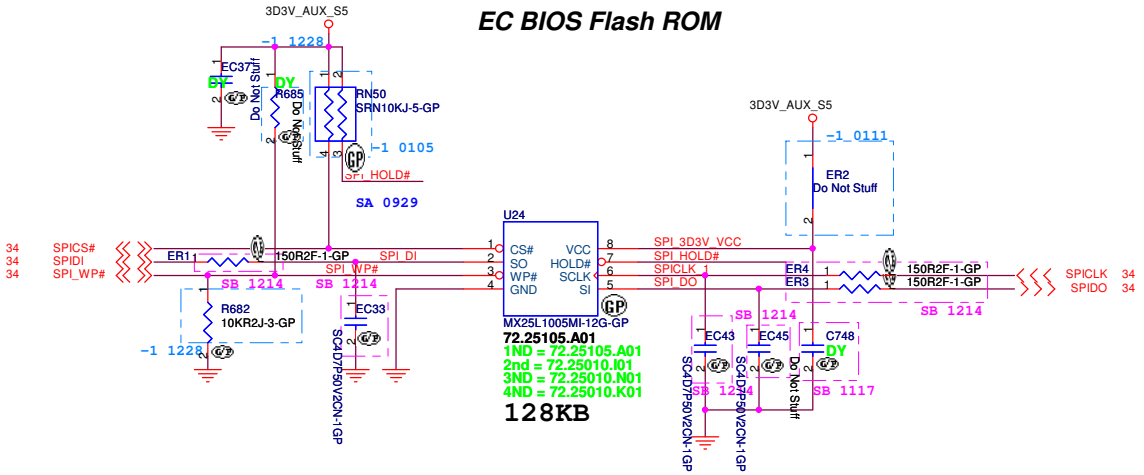
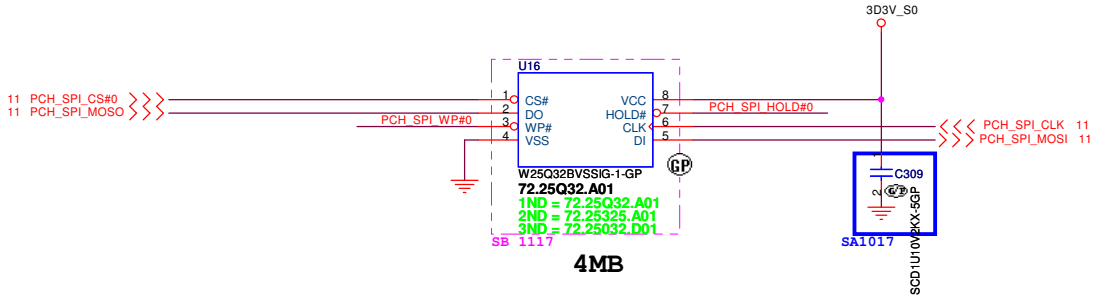
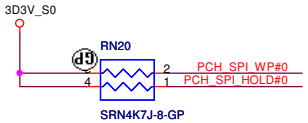
EC BIOS Flash ROM

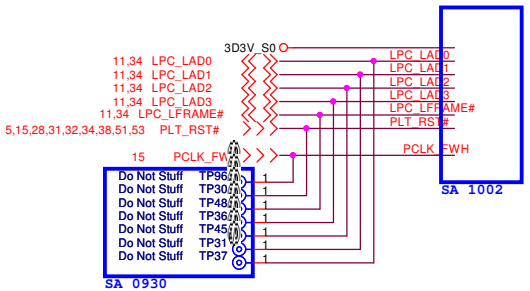


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



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Title: **BIOS**

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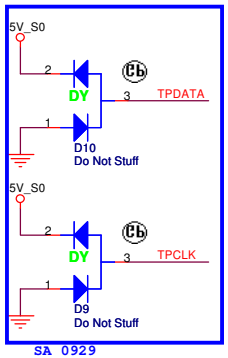
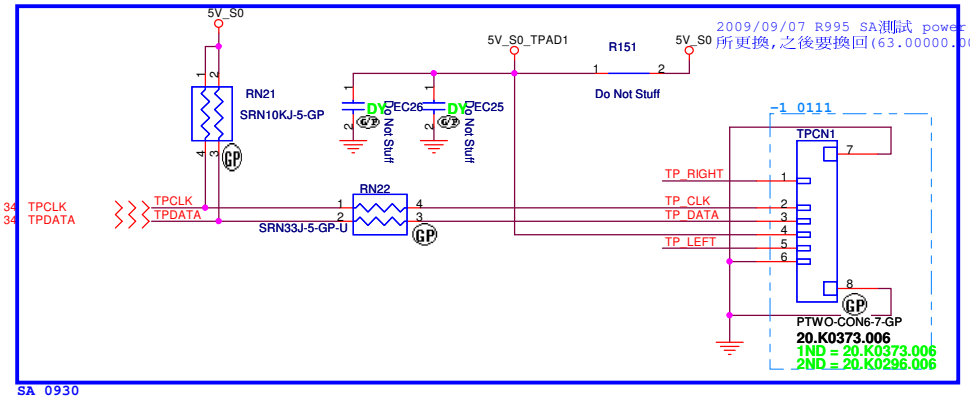
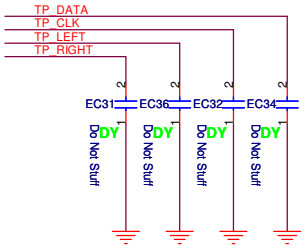
TOUCH PAD







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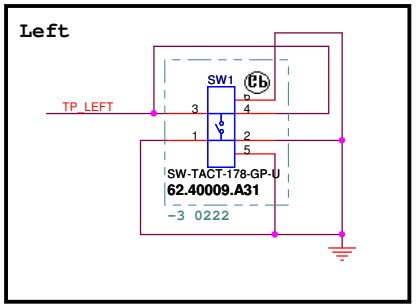
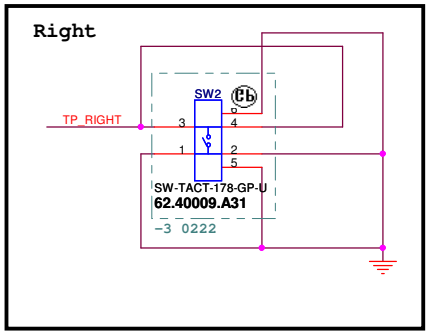
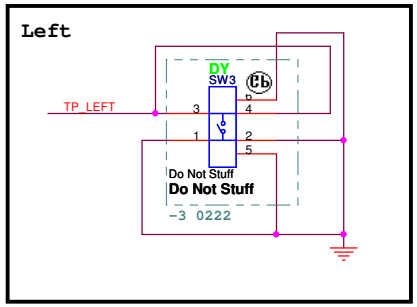
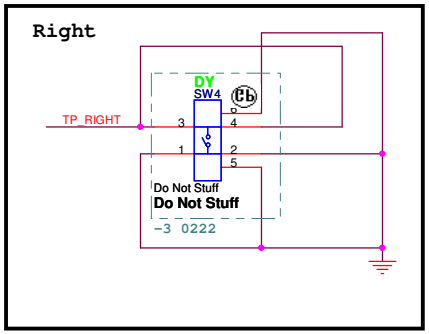
T/P









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Title		
Touch PAD		
Size A3	Document Number JM31-CP	Rev -1
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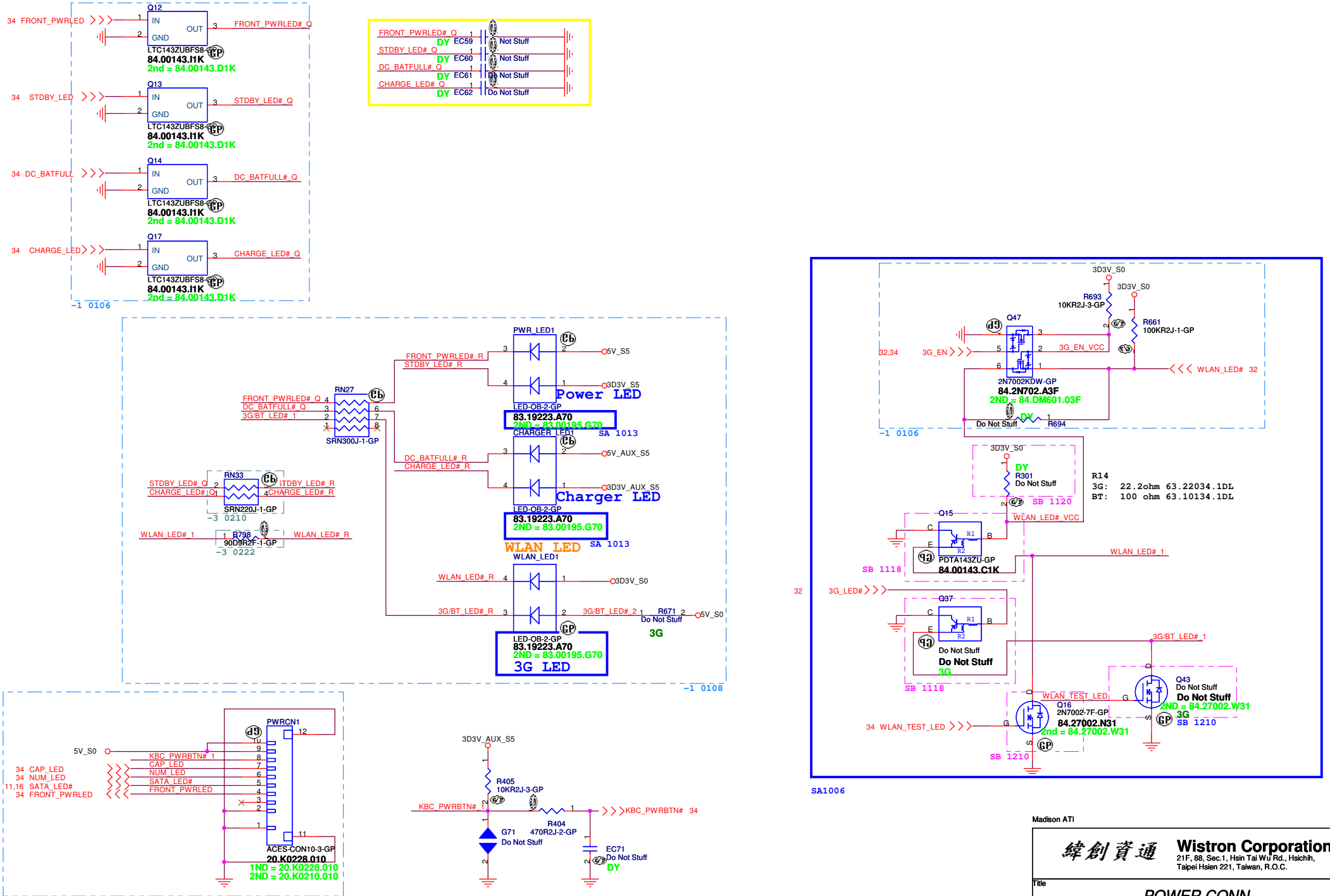

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Title	POWER CONN	
Size A3	Document Number JM31-CP	Rev -3
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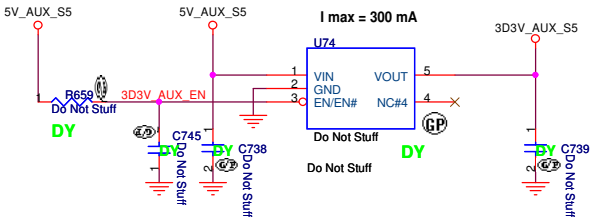
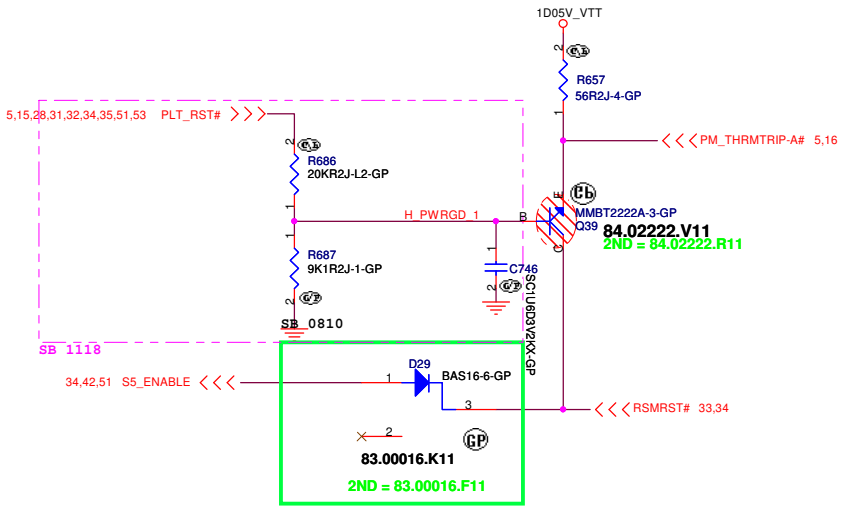
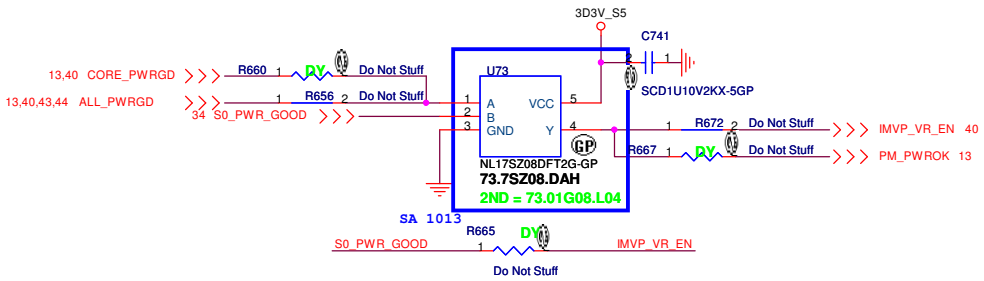
Run Power

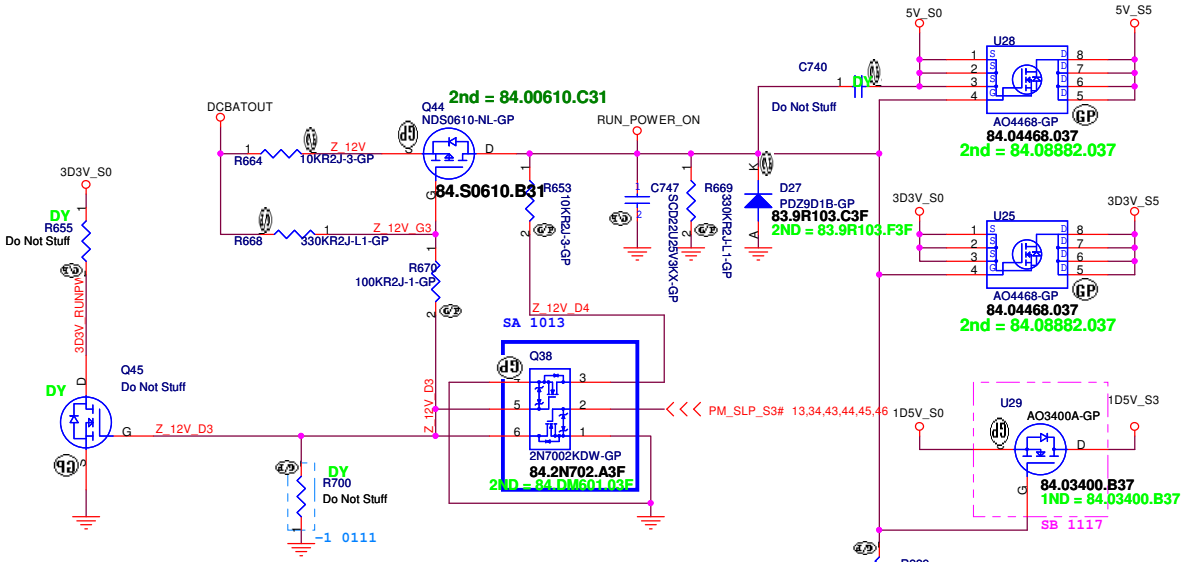
Aux Power

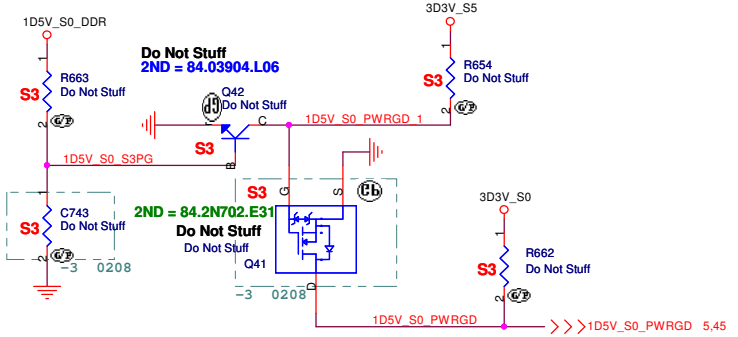
3D3V_AUX_S5











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Title	***RUN POWER and 3D3V_AUX_S5***
Size A3 / Document Number	JM31-CP / Rev -3
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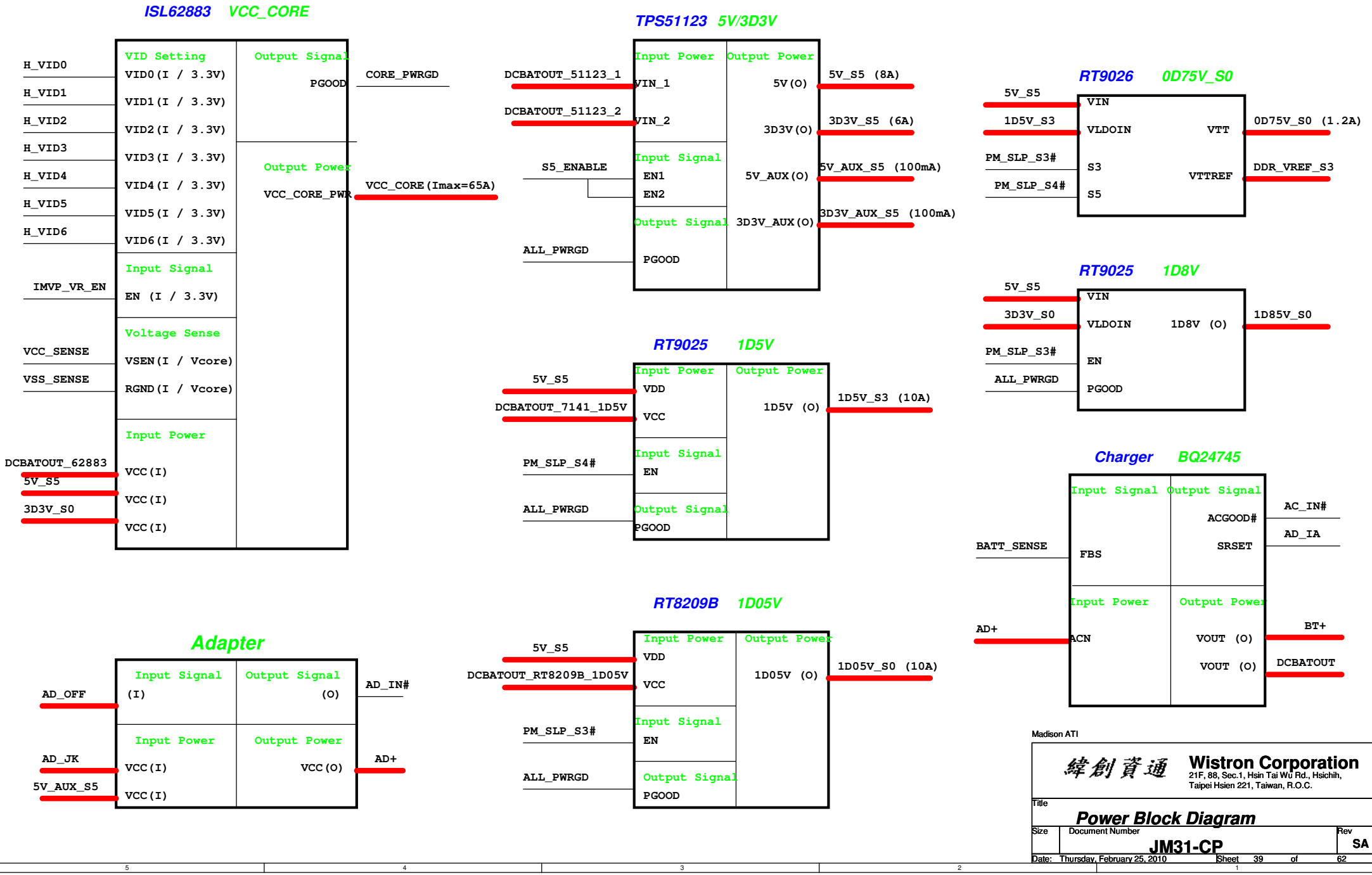

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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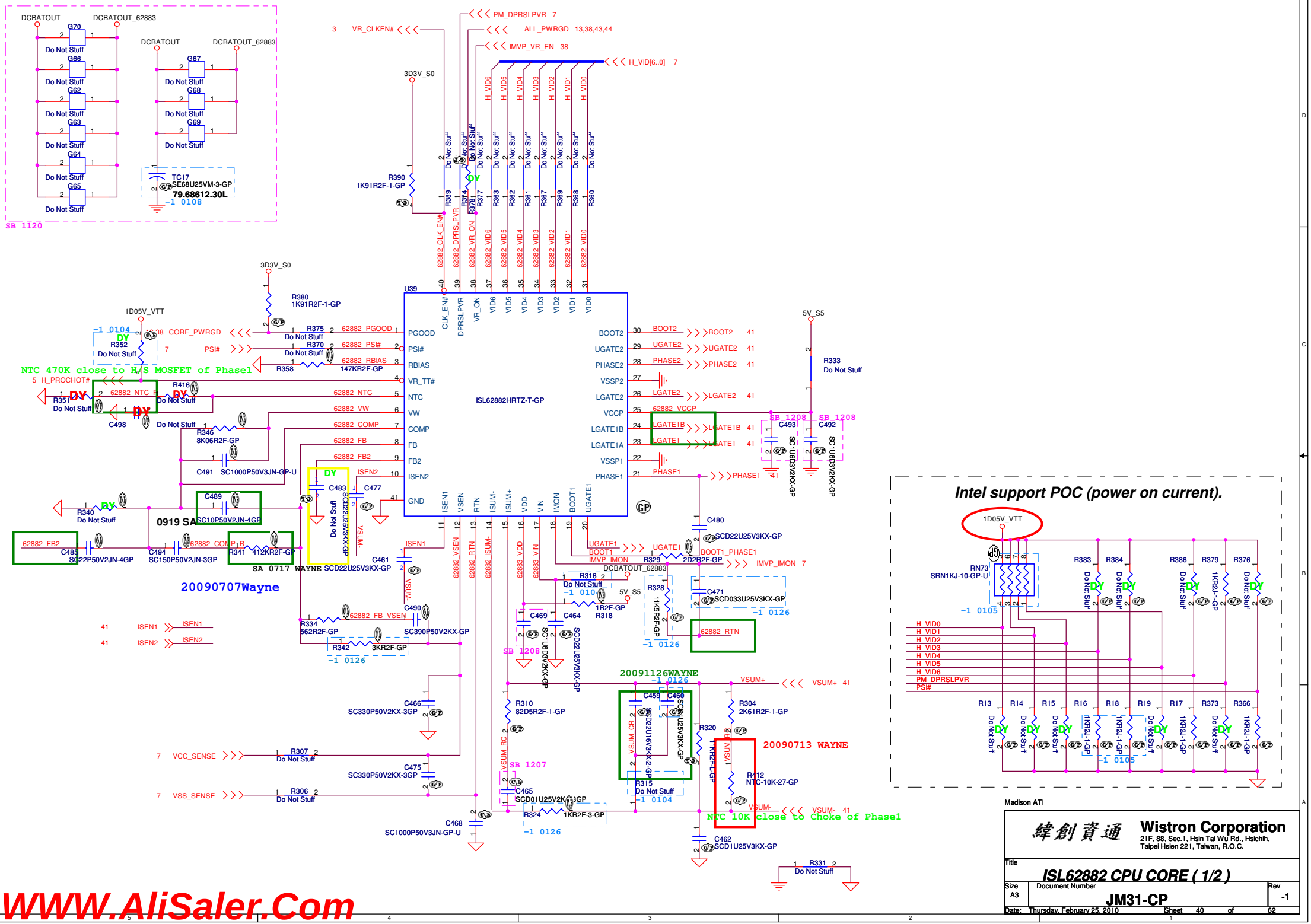

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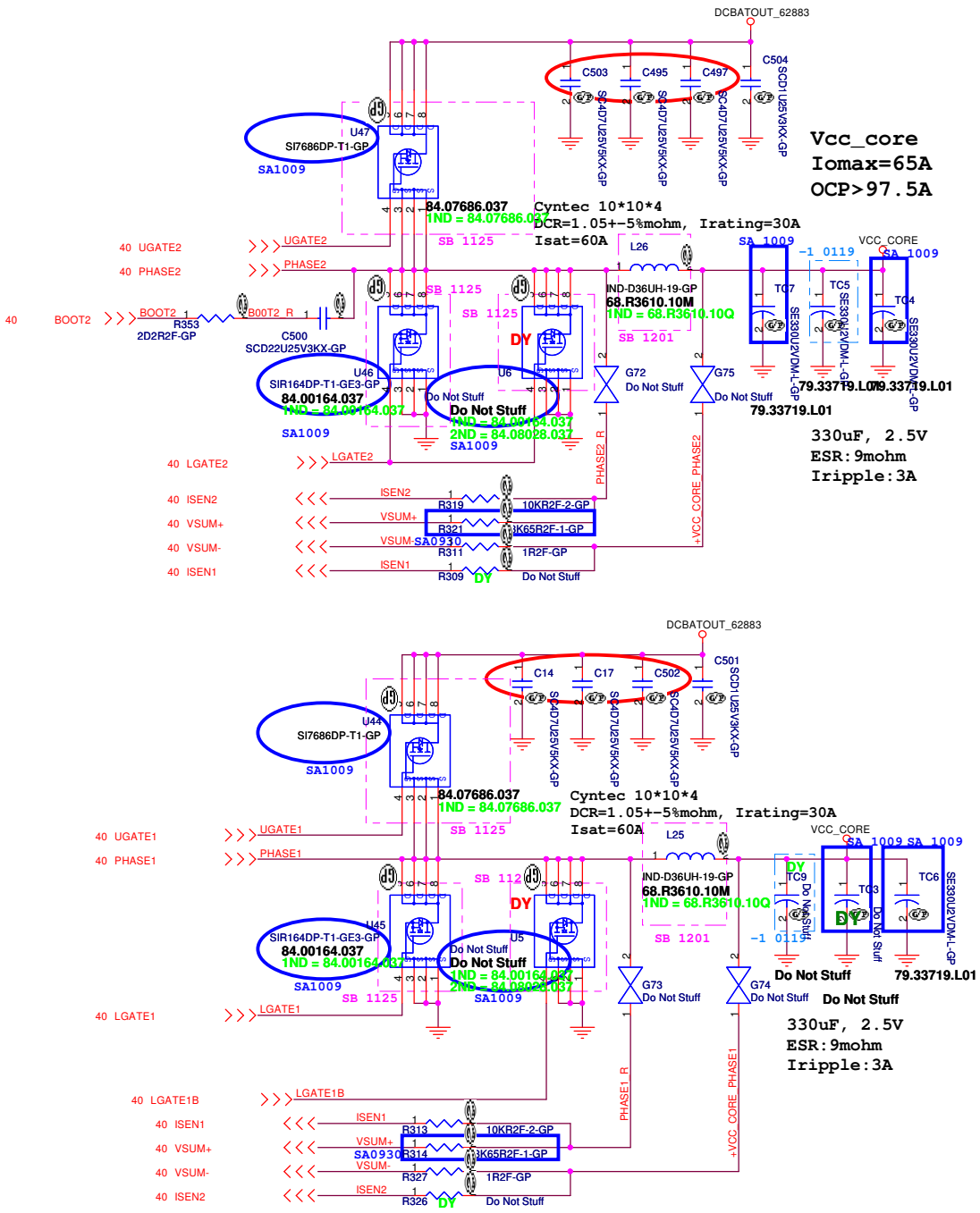

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Title: *ISL62882 CPU CORE (2/2)*

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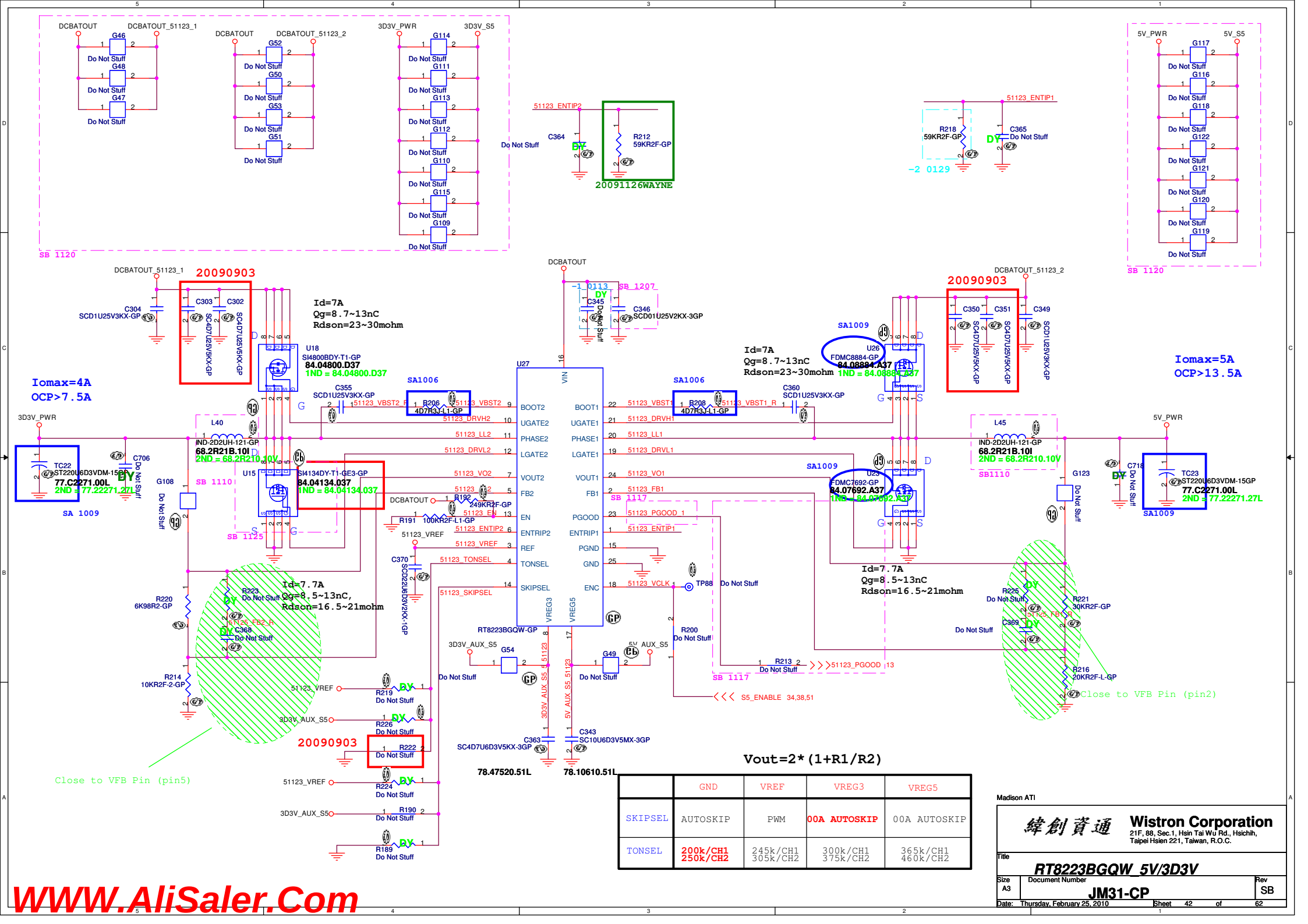

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223BGQW_5V/3D3V

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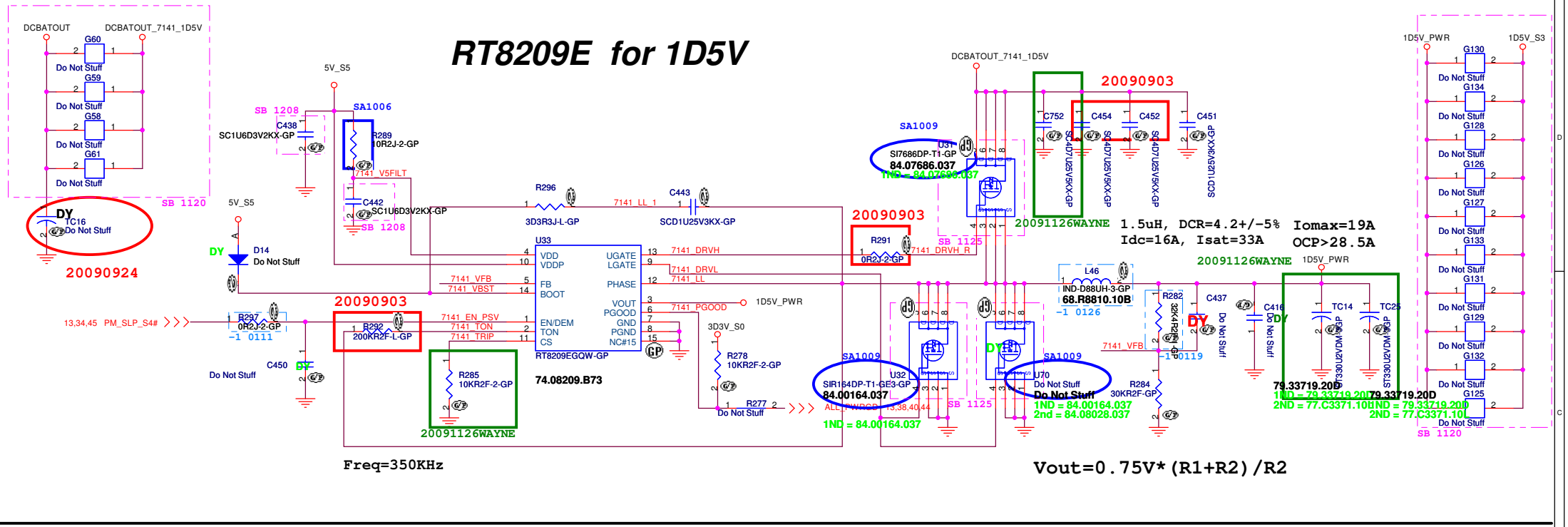
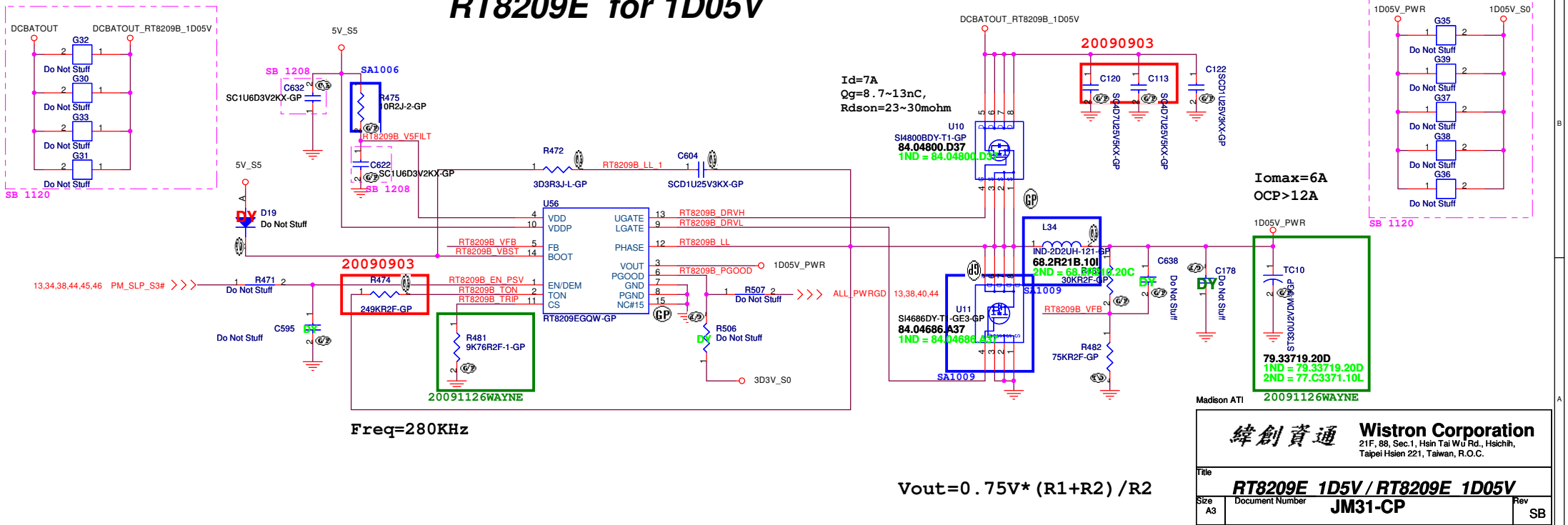
RT8209E for 1D5V



RT8209E for 1D05V



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Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT8209E 1D5V / RT8209E 1D05V*	
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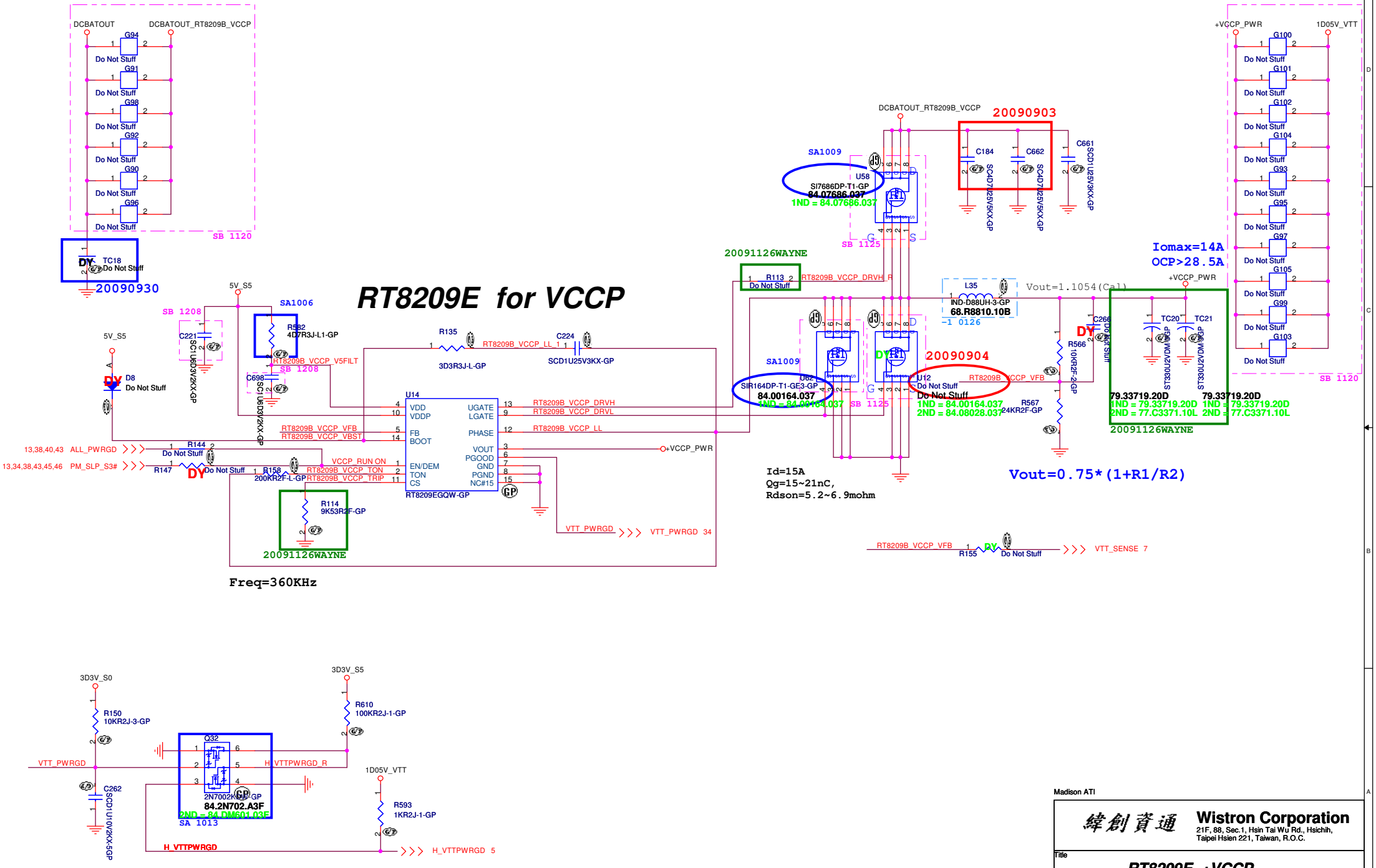
RT8209E for VCCP



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209E +VCCP**

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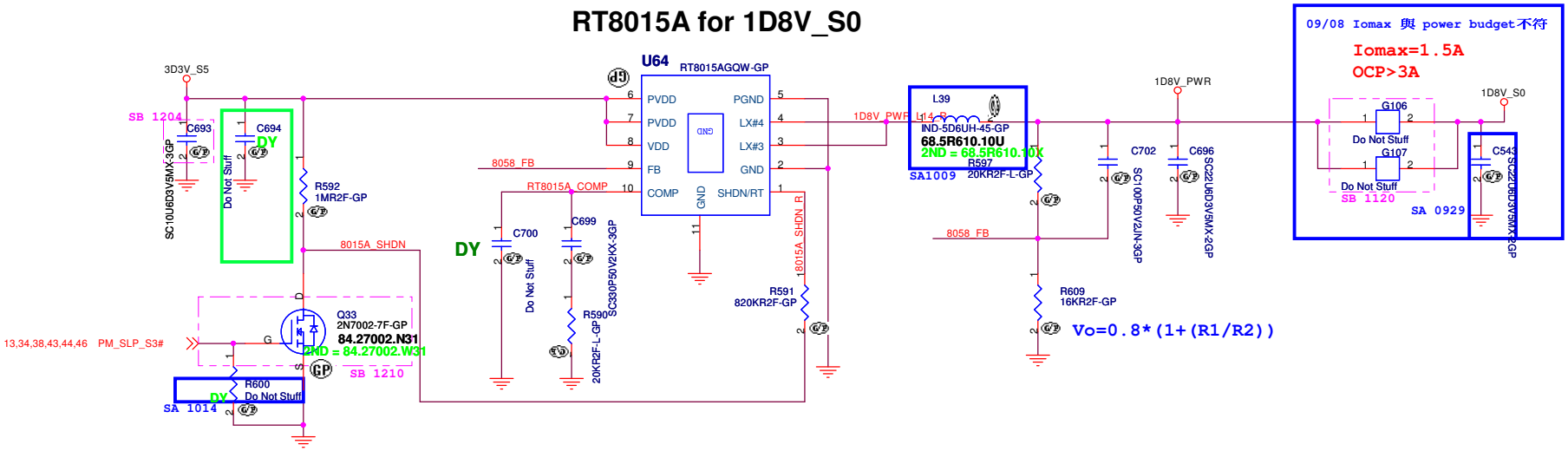
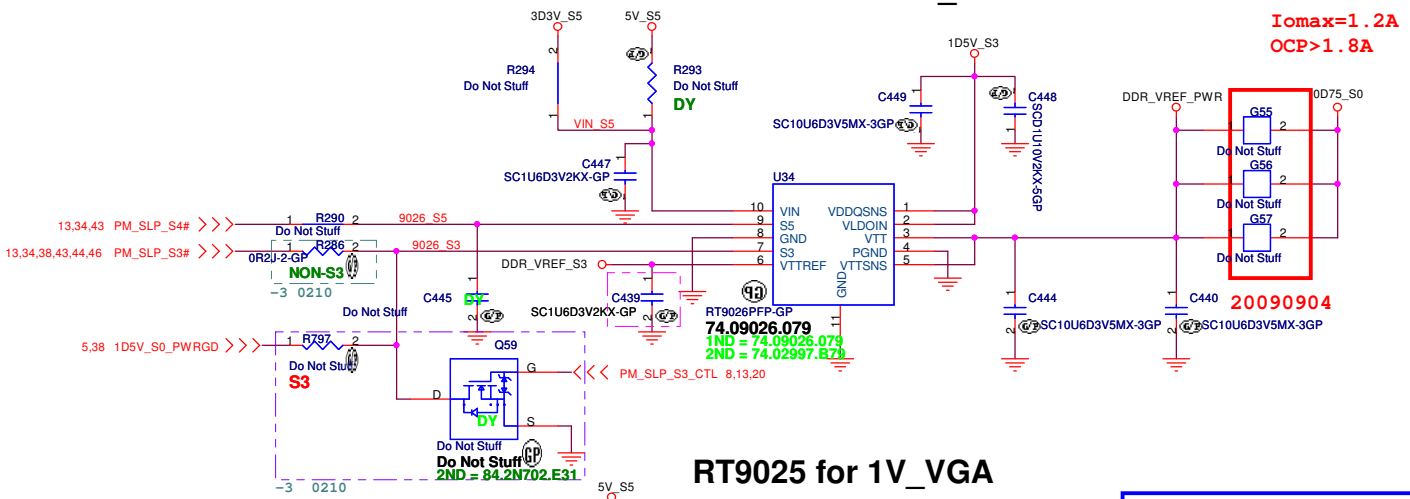
RT8015A for 1D8V_S0

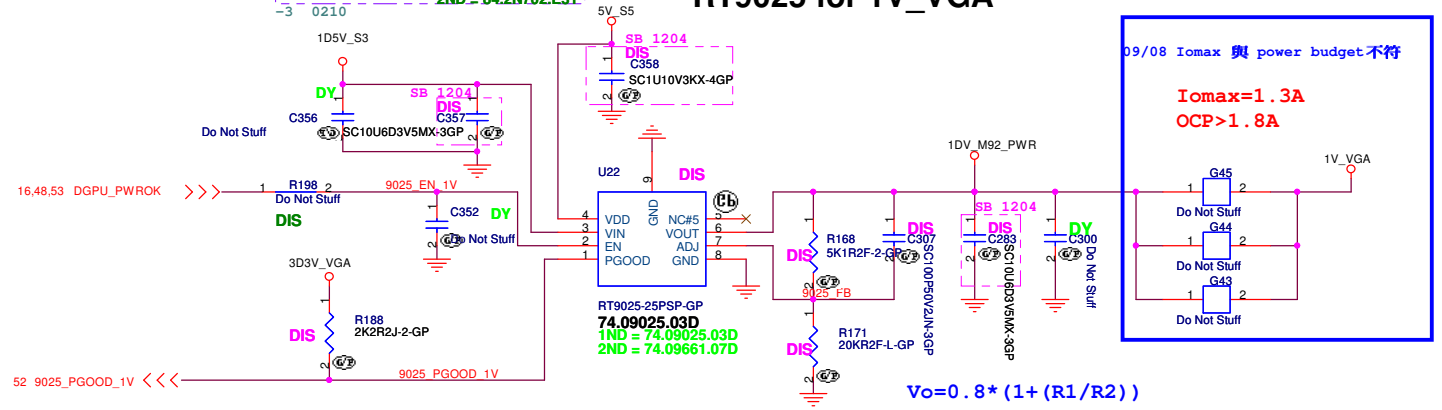


09/08 add 3D3V_S5,R837,R836

RT9026 for 0D75V_S3



RT9025 for 1V_VGA



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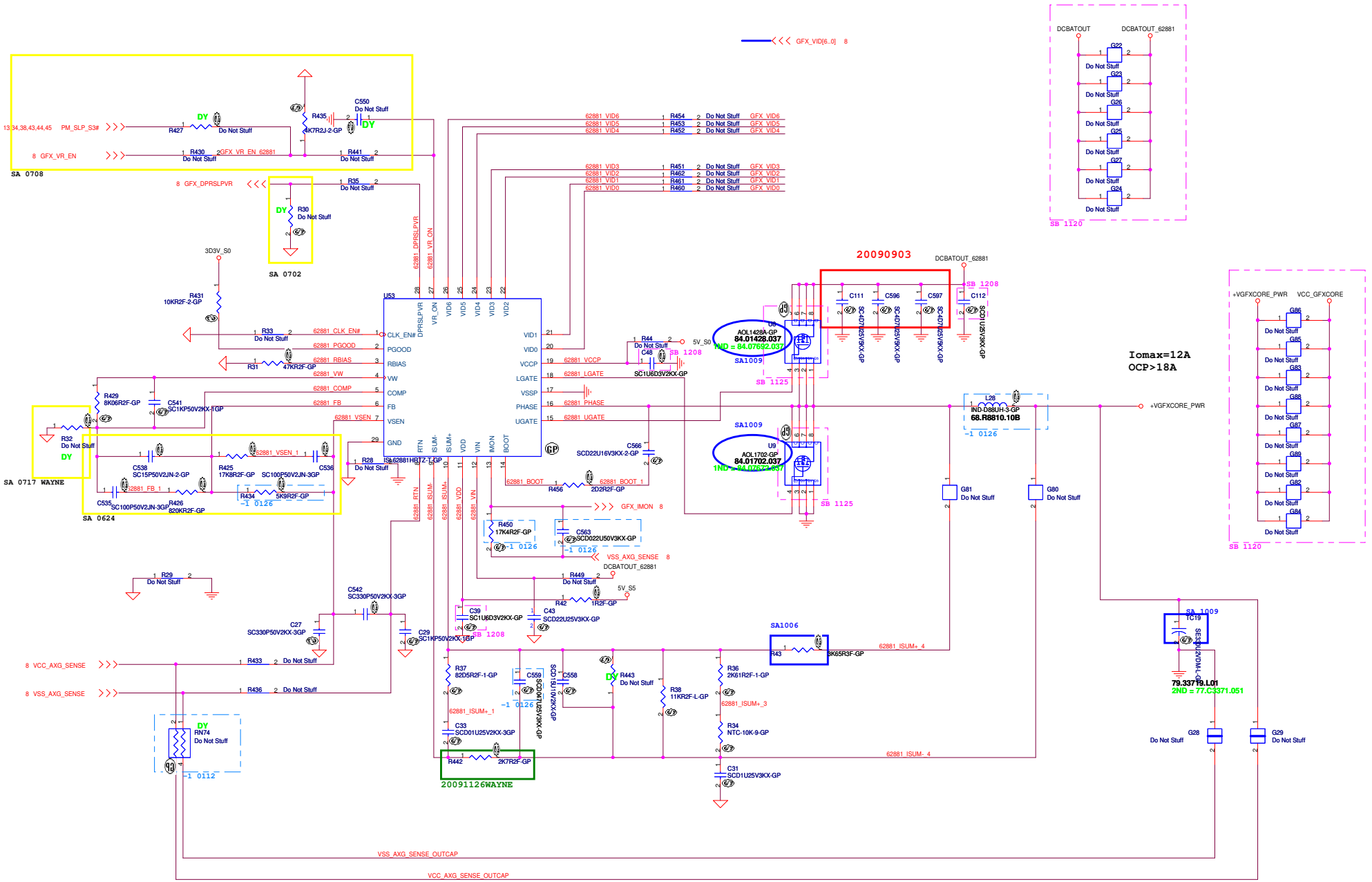
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V_1V/RT9026_0D75

Size	Document Number	Rev
A3	JM31-CP	-3

Date: Thursday, February 25, 2010 Sheet 45 of 62



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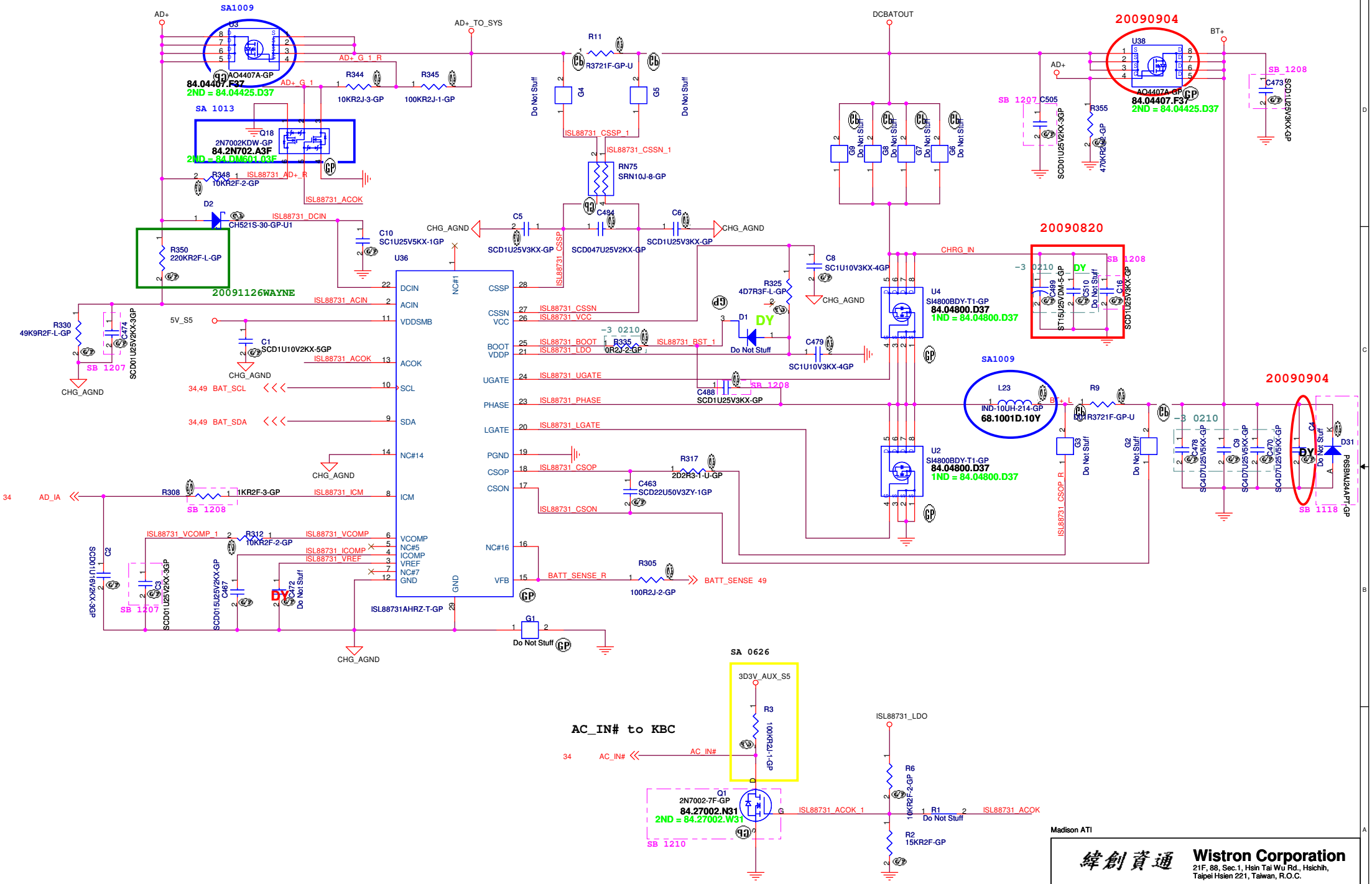
Title: ISL62881_+VCC_GFXCORE

Size	Document Number	Rev
C	JM31-CP	SB

Date: Thursday, February 25, 2010 Sheet 46 of 62



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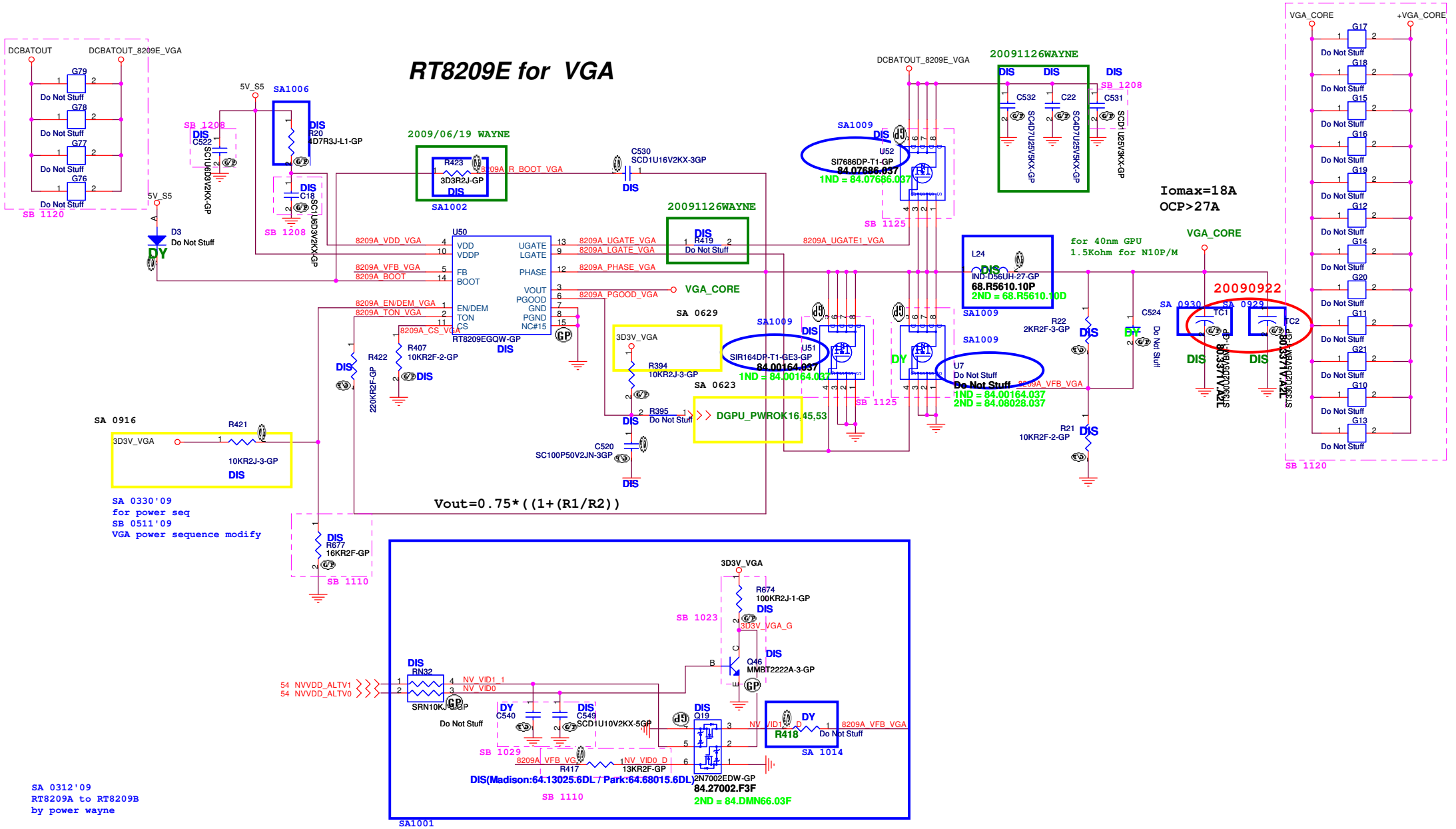
Title: *ISL88731A_CHARGER*

Size	Document Number	Rev
A3	JM31-CP	-3

Date: Thursday, February 25, 2010 Sheet 47 of 62

RT8209E for VGA



PARK (6.8K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

MADISON (13K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

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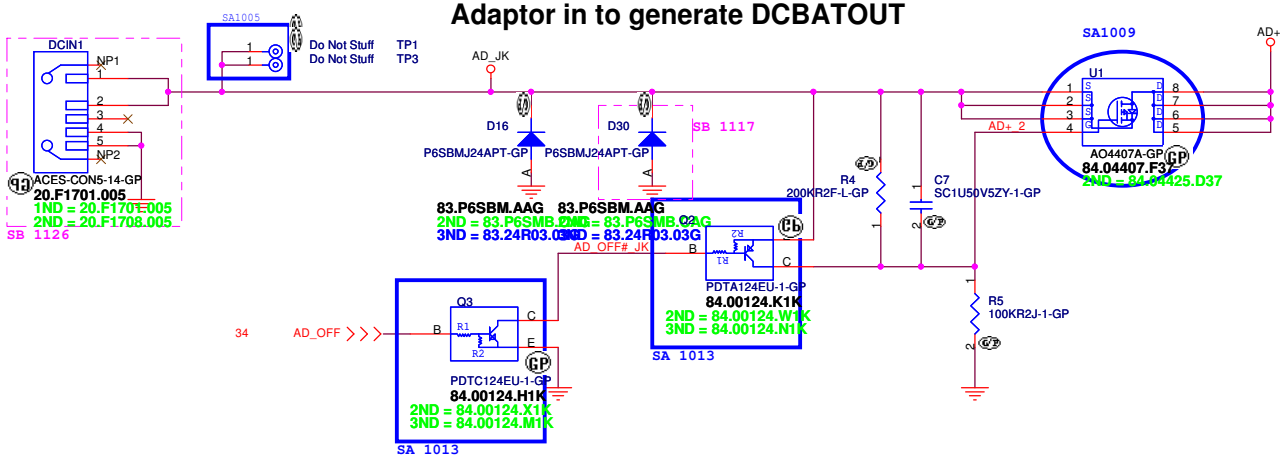
Title: RT8209E_VGA_CORE

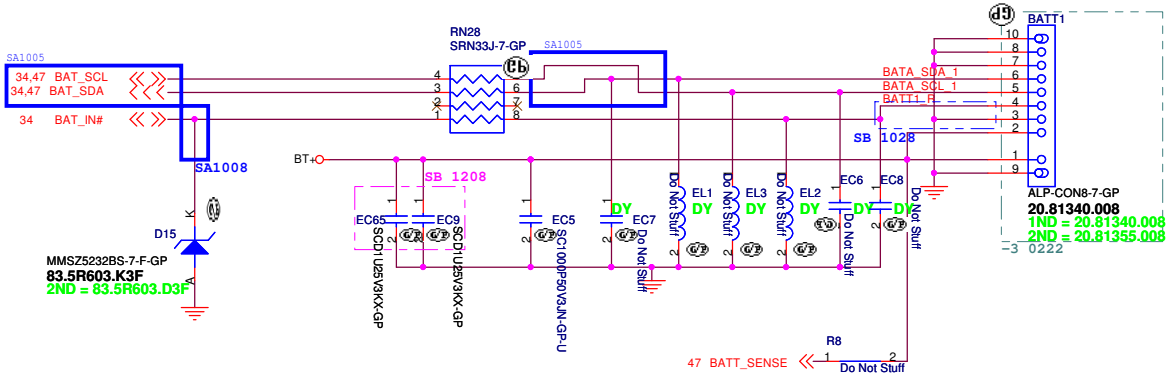
Size: A3 | Document Number: JM31-CP | Rev: SB

Date: Thursday, February 25, 2010 | Sheet 48 of 62

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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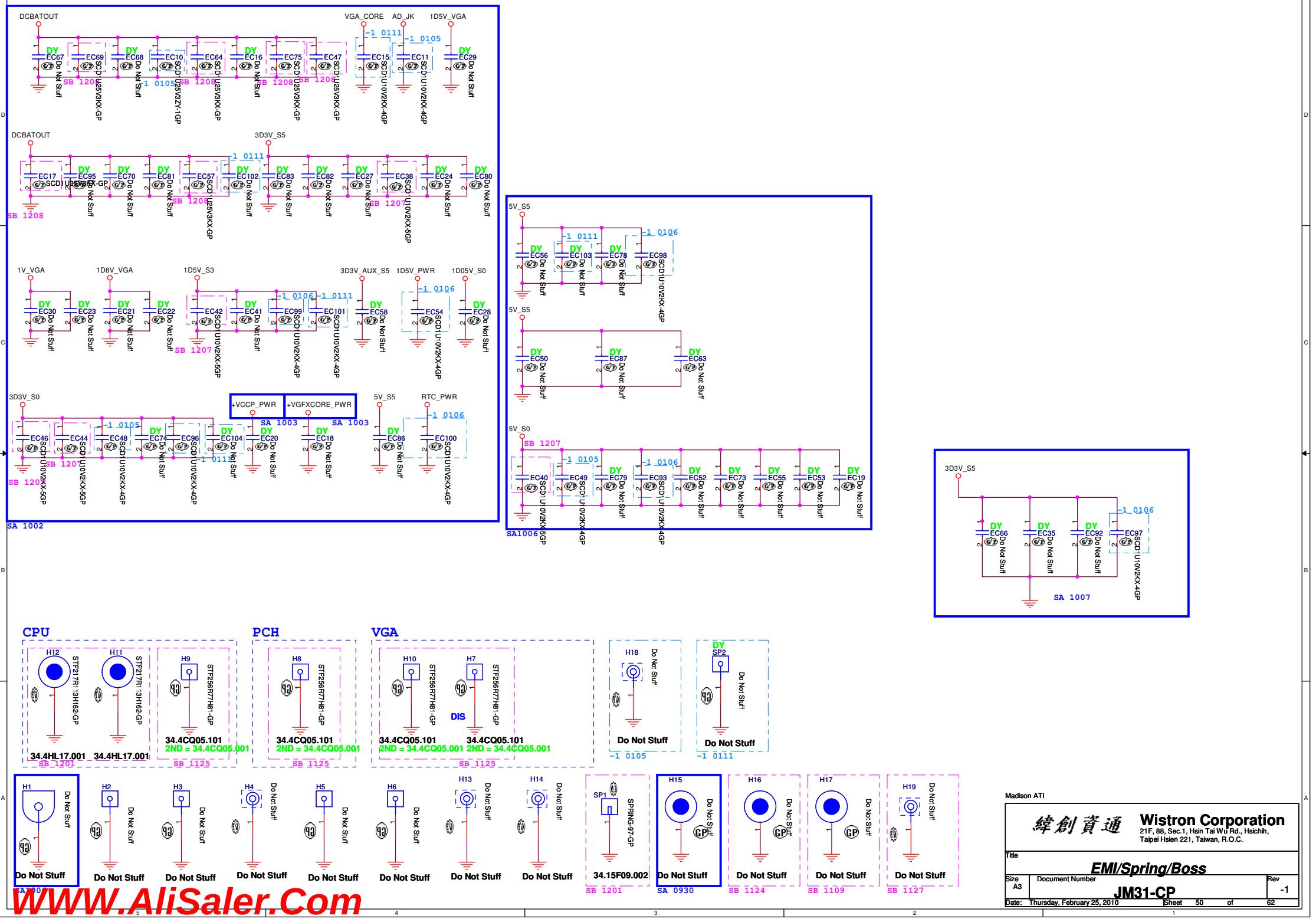
Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	JM31-CP	SB

Date: Thursday, February 25, 2010 Sheet 49 of 62



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Title: EMI/Spring/Boss

Size	Document Number	Rev
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Date: Thursday, February 25, 2010 Sheet 50 of 62

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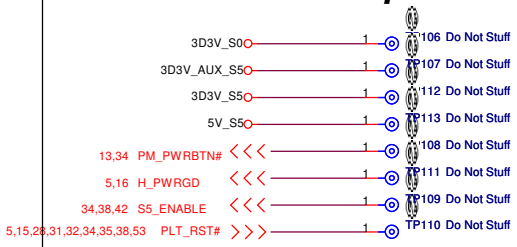
Check test point



Test Point放在Dimm Door打開可量測處

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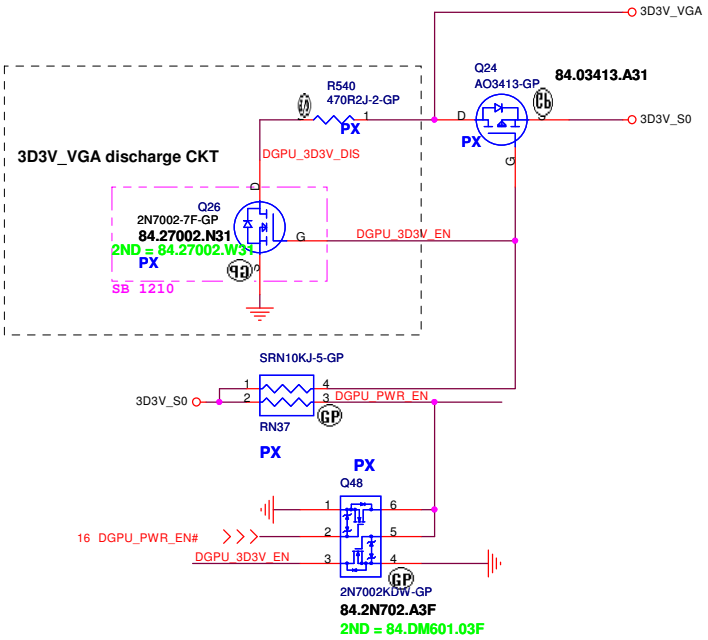
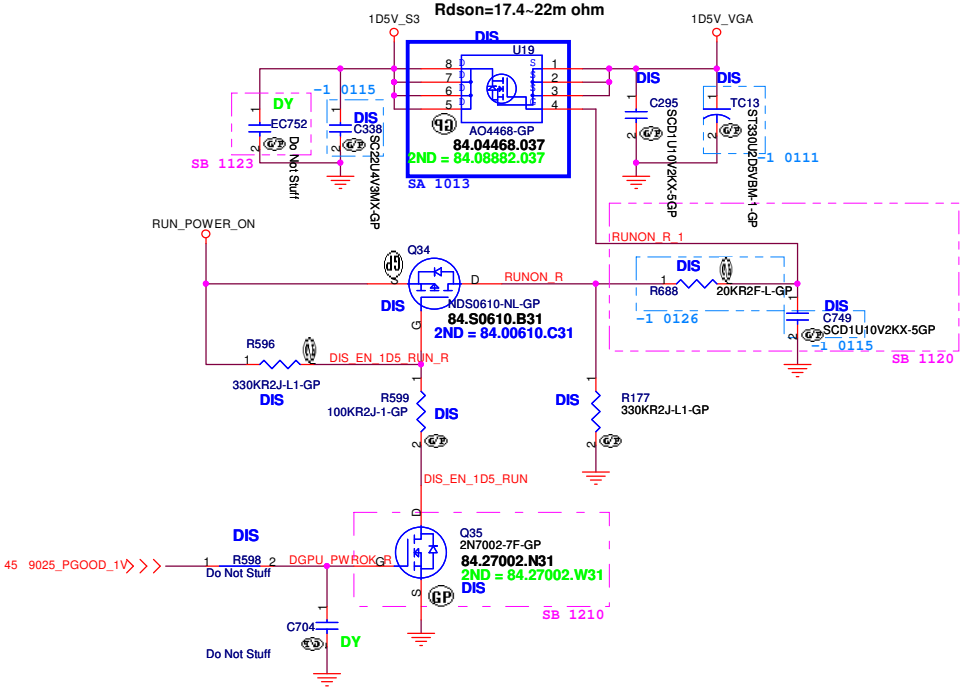
Title		
AFTE_TP		
Size: A3	Document Number: JM31-CP	Rev: SA
Date: Thursday, February 25, 2010	Sheet 51 of 62	

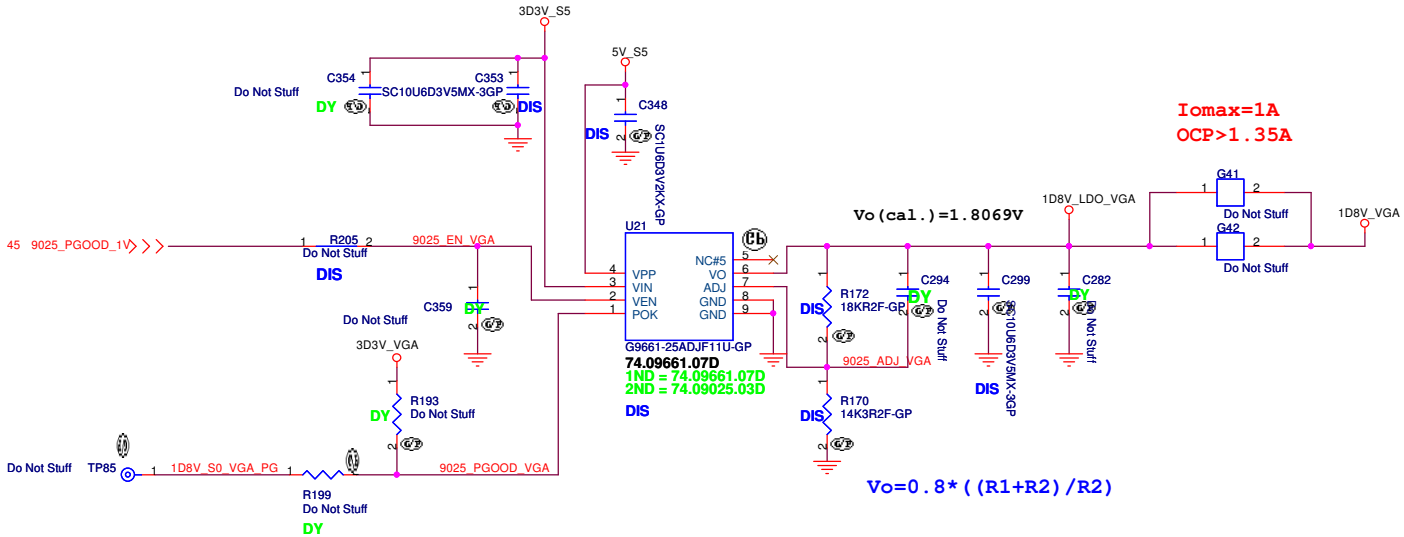
+3VS to 3.3V_DELAY Transfer



AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



G9661 for 1D8V_VGA



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Title: **ATI_POWER**

Size	Document Number	Rev
A3	JM31-CP	-1

Date: Thursday, February 25, 2010 Sheet 52 of 62

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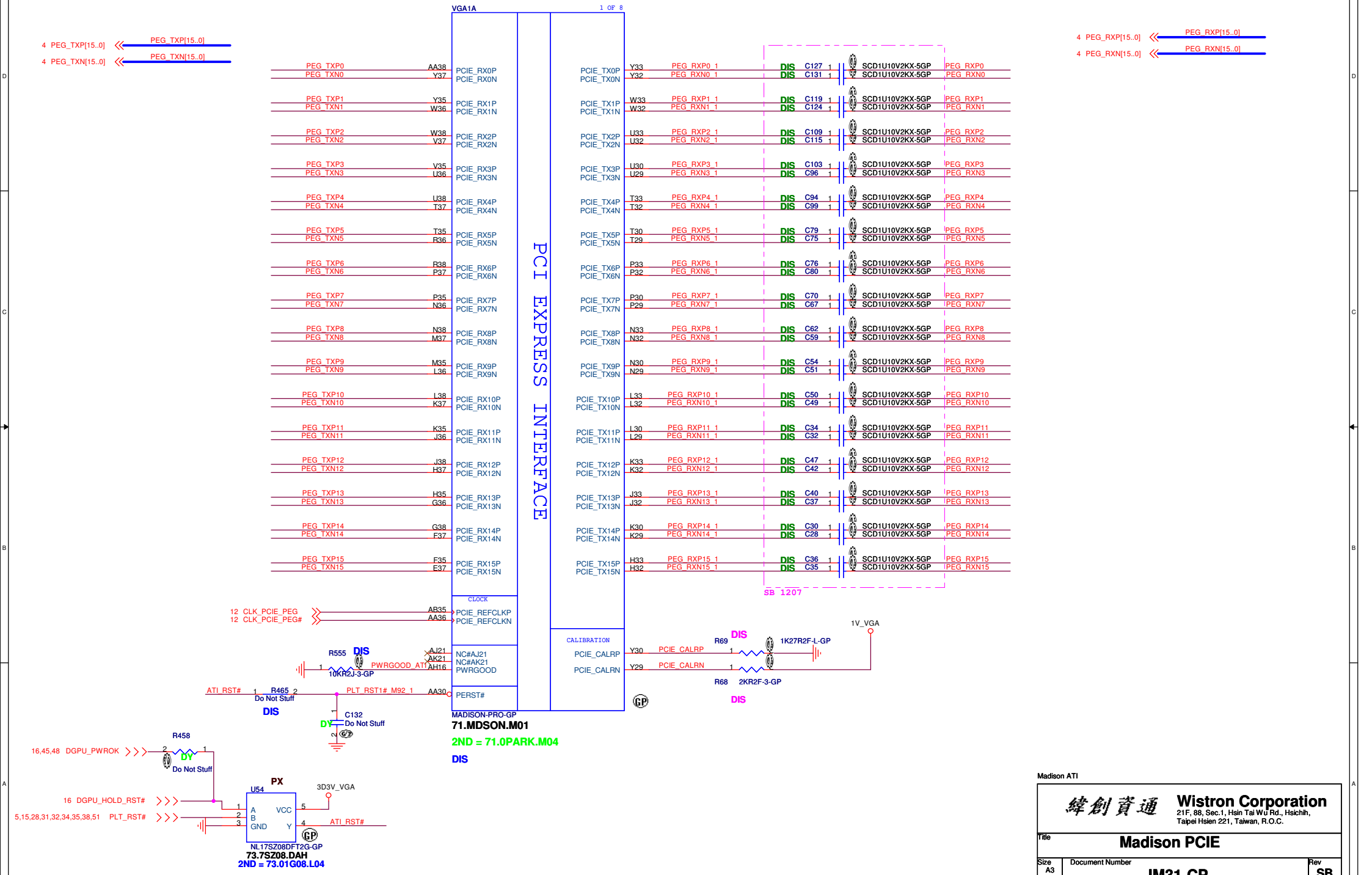

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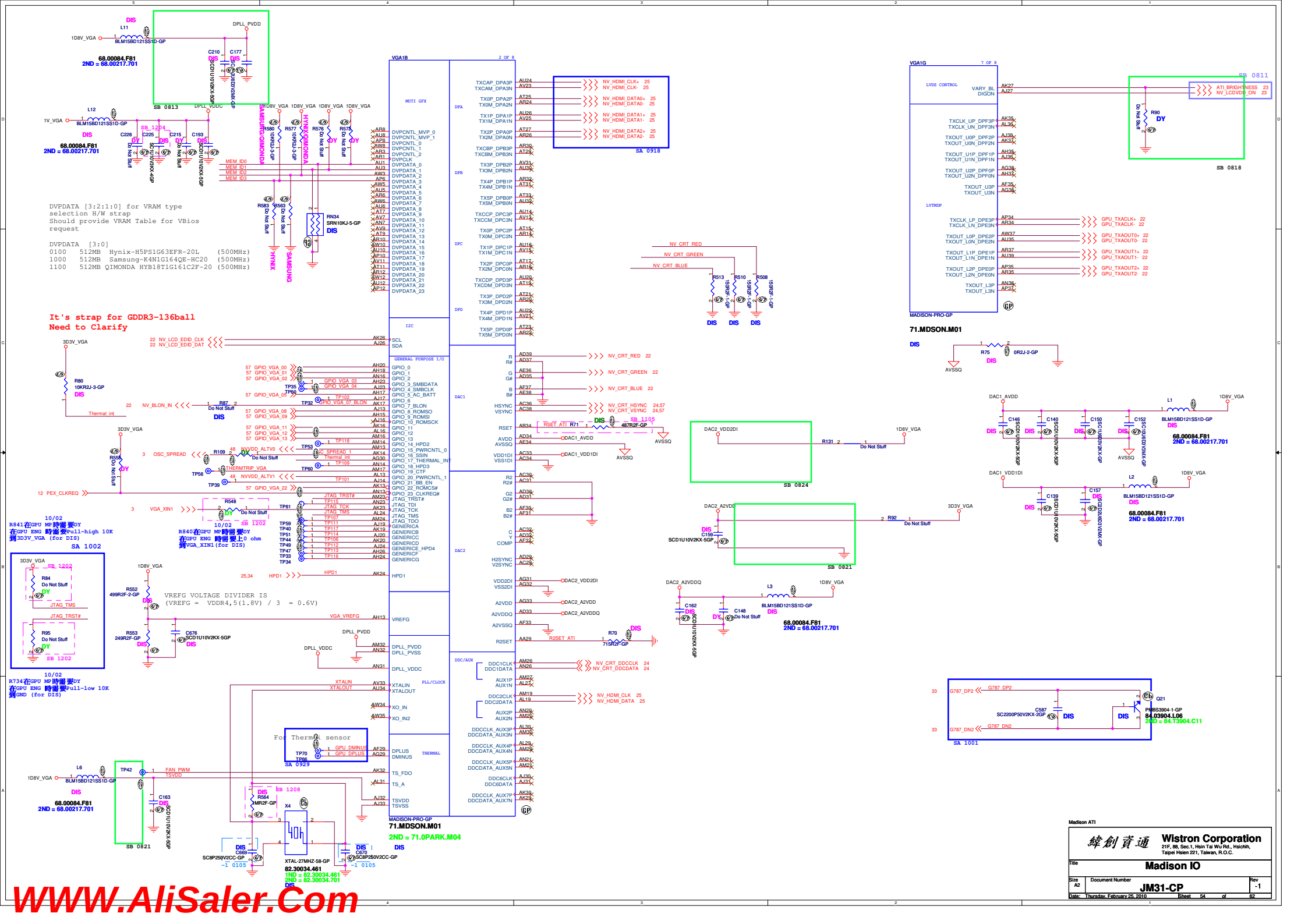
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Madison PCIE	
Size: A3	Document Number: JM31-CP
Rev: SB	
Date: Thursday, February 25, 2010	Sheet 53 of 62


DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
VGA1B
VGA1G
MADISON-PRO-GP
71.MDSON.M01
2ND = 71.0PARK.M04
SA 0813
SA 0918
SA 0818
SA 0824
SA 0821
SA 1002
SA 0929
SA 1001
SB 0811
SB 0821
SB 1202
SB 1204
SB 1208
SB 1105
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Madison ATI
Madison IO
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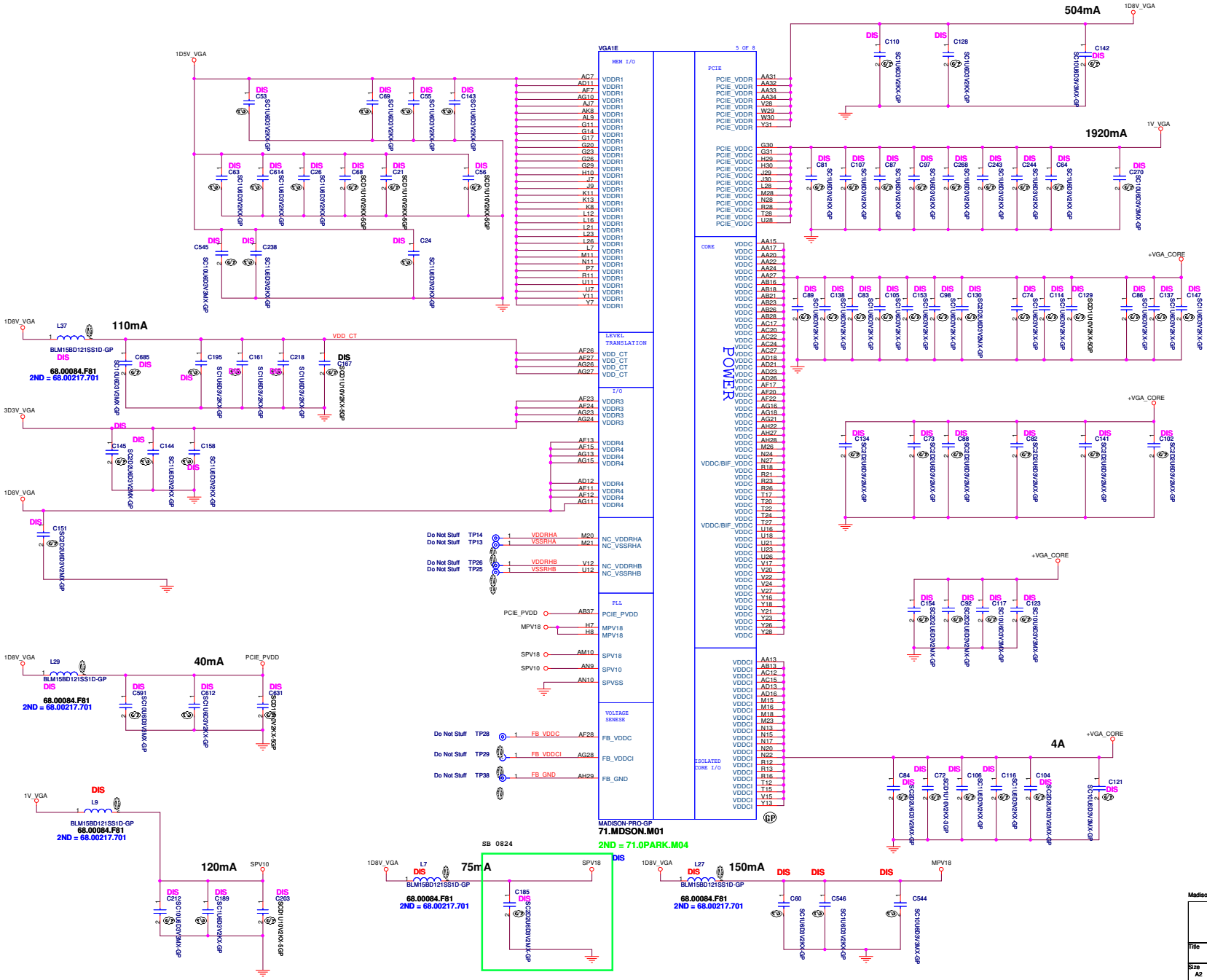

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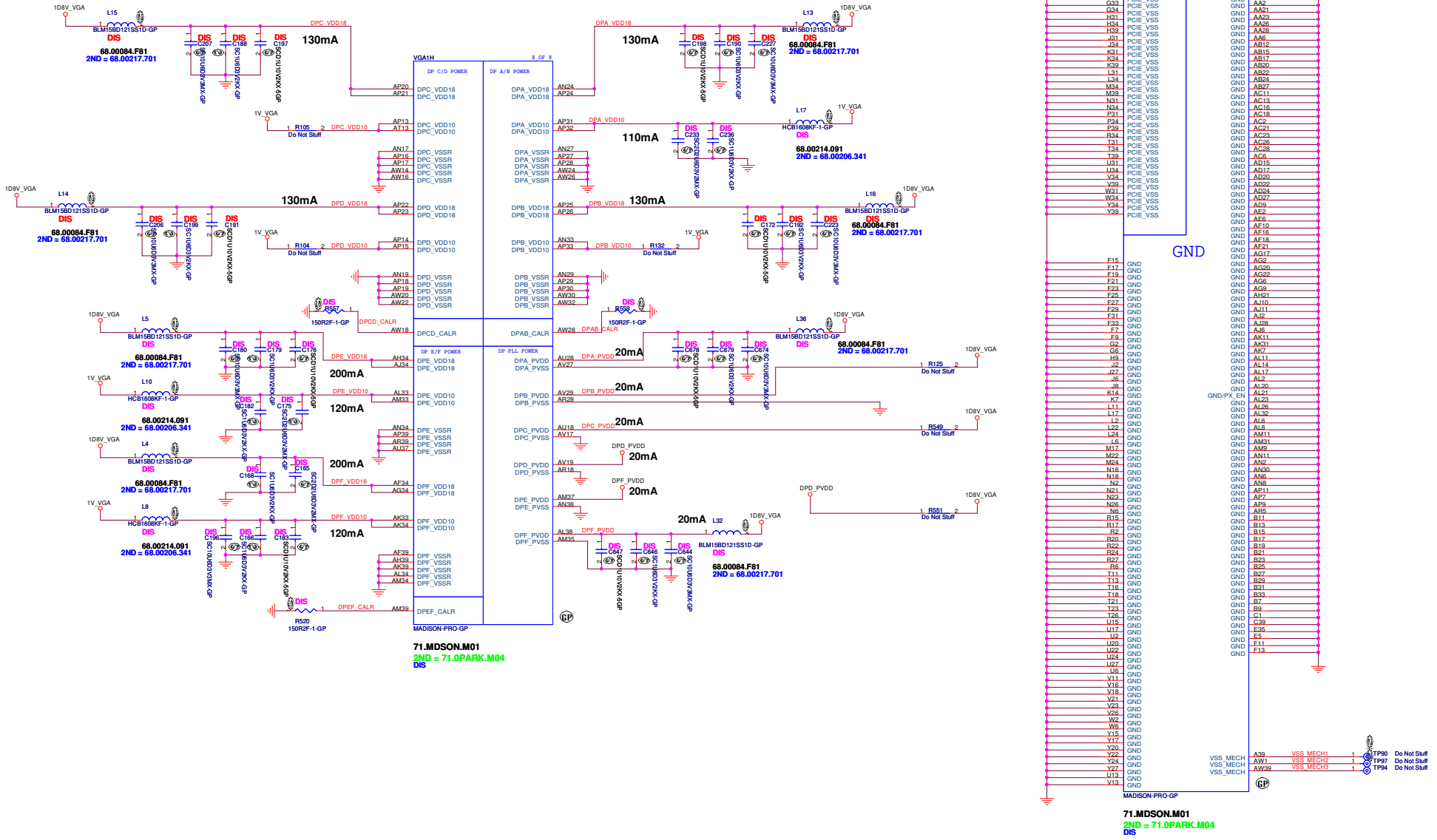
Title	Madison POWER	
Size A2	Document Number JM31-CP	Rev SB
Date: Thursday, February 25, 2010	Sheet 55 of 62	



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Title	DP POWER_GND	
Size: A2	Document Number: JM31-CP	Rev: SB
Date: Thursday, February 25, 2010	Sheet 56 of 62	

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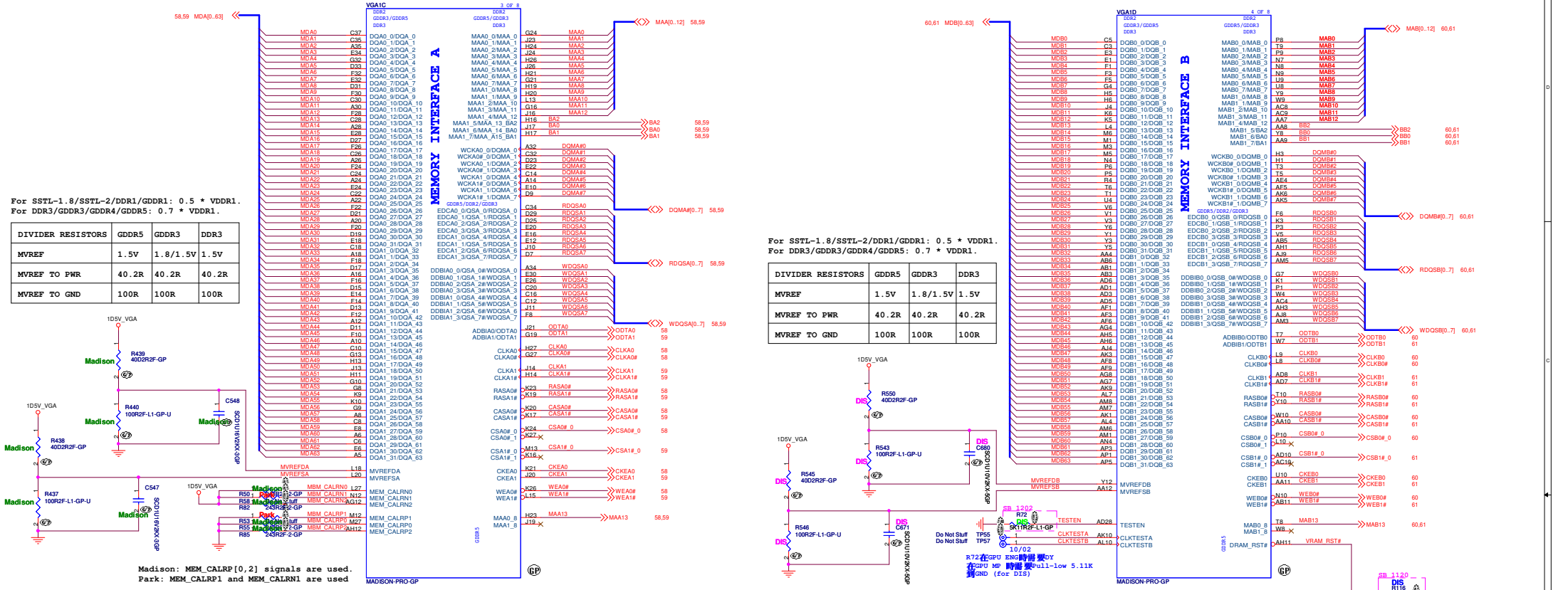

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Title: Madison Memory / Straps

Size: A2 | Document Number: JM31-CP | Rev: SB

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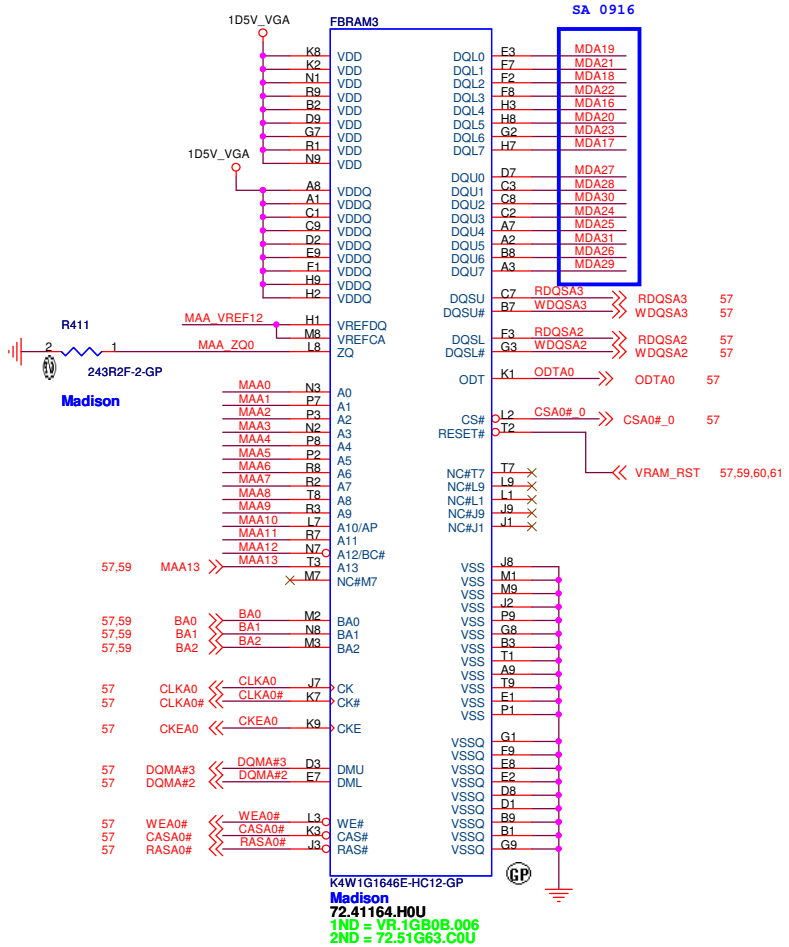
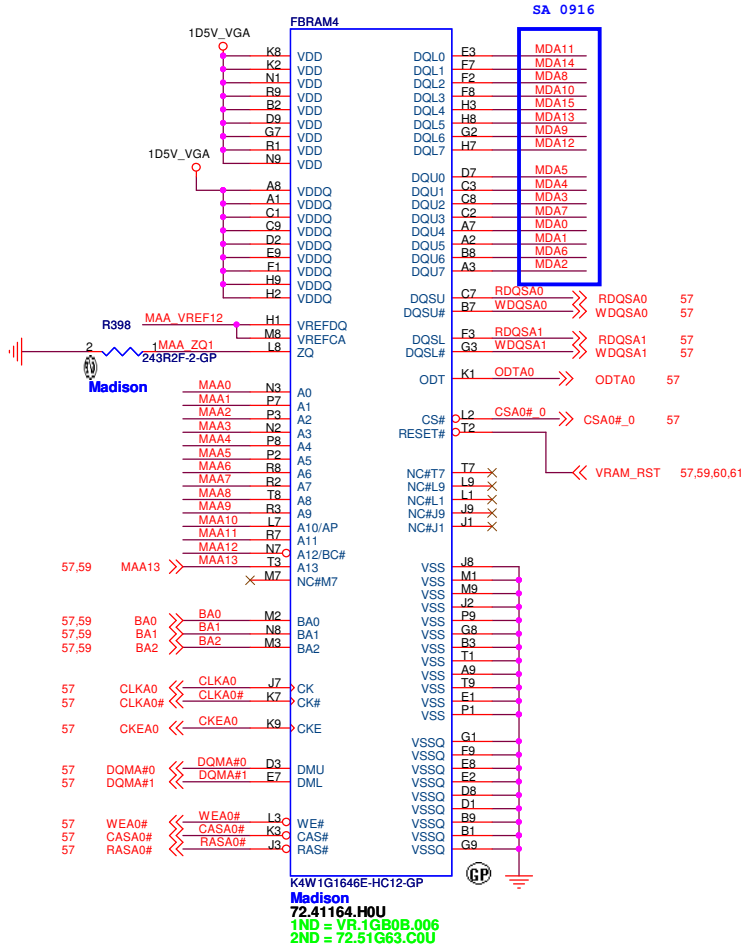
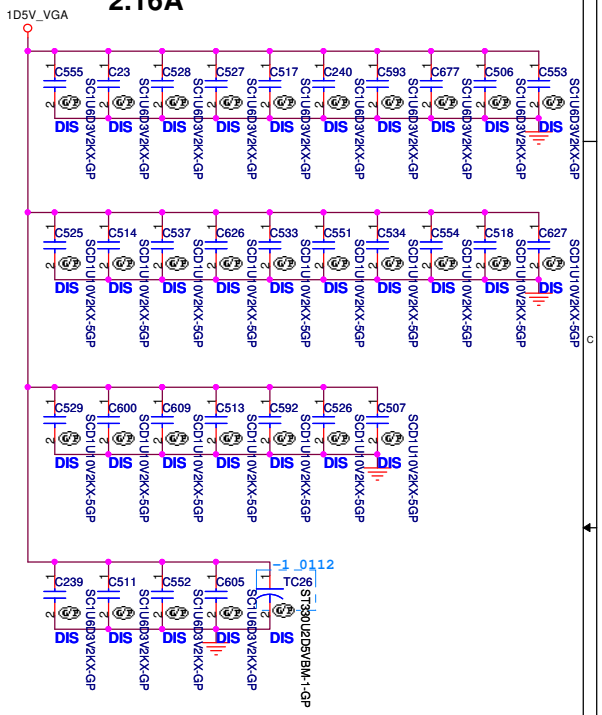
DDR3







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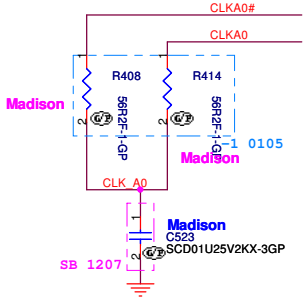
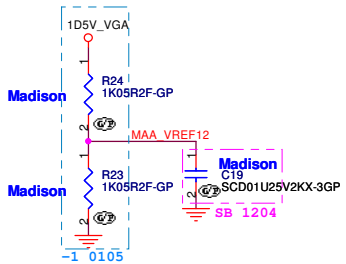
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





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57,59 RDQSA[0..7]
57,59 WDQSA[0..7]
57,59 MAA[0..12] MAA[0..12]
57,59 MDA[0..63] MDA[0..63]

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Title	VRAM(1/4)	
Size A3	Document Number JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 58 of 62	

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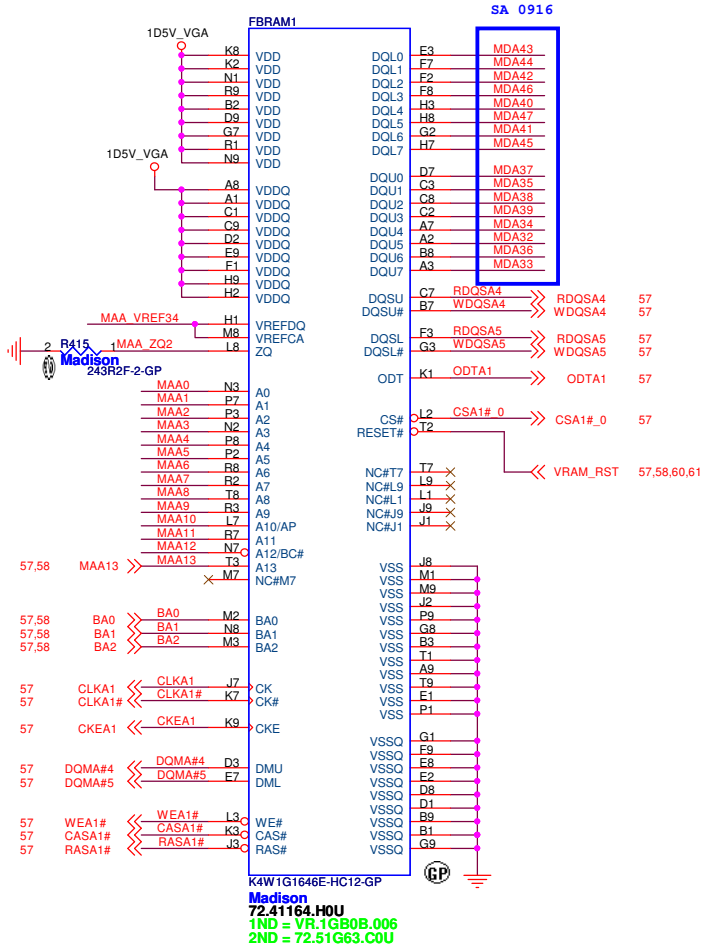
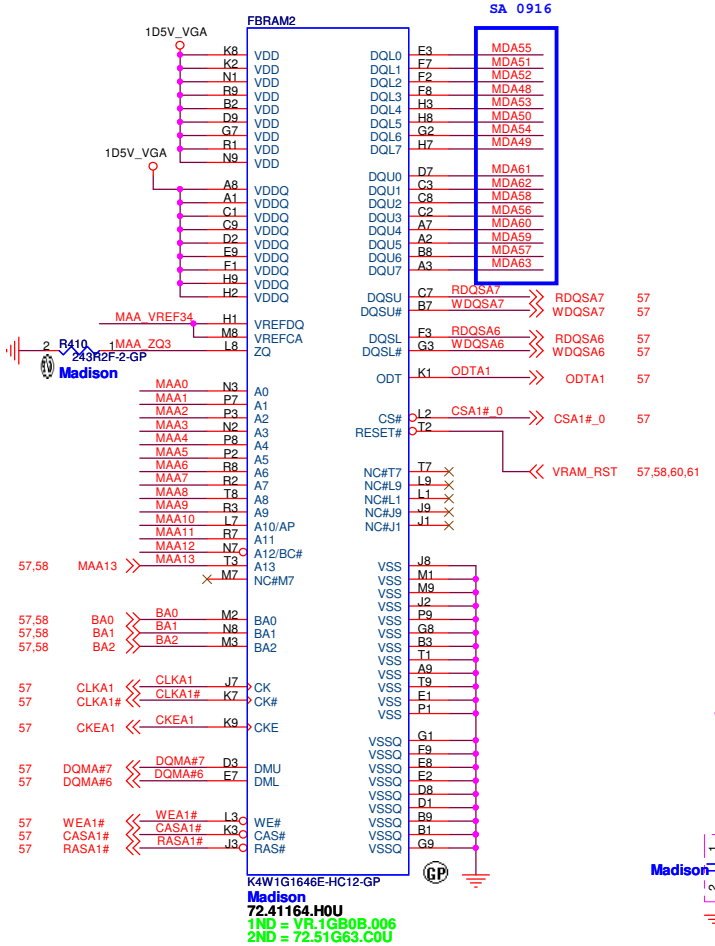
DDR3





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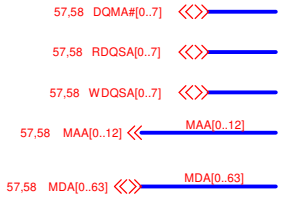

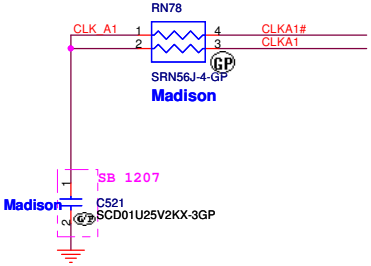

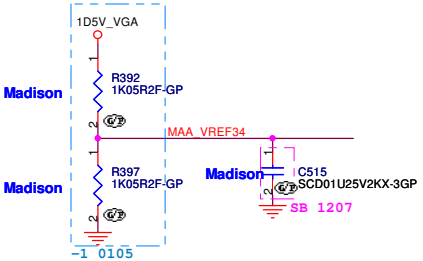

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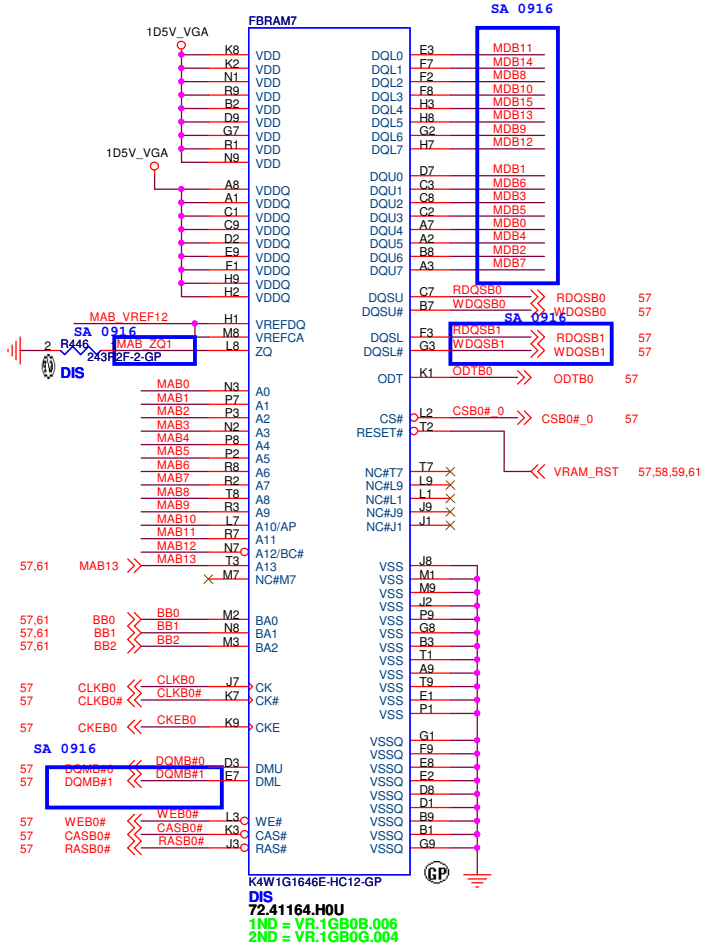
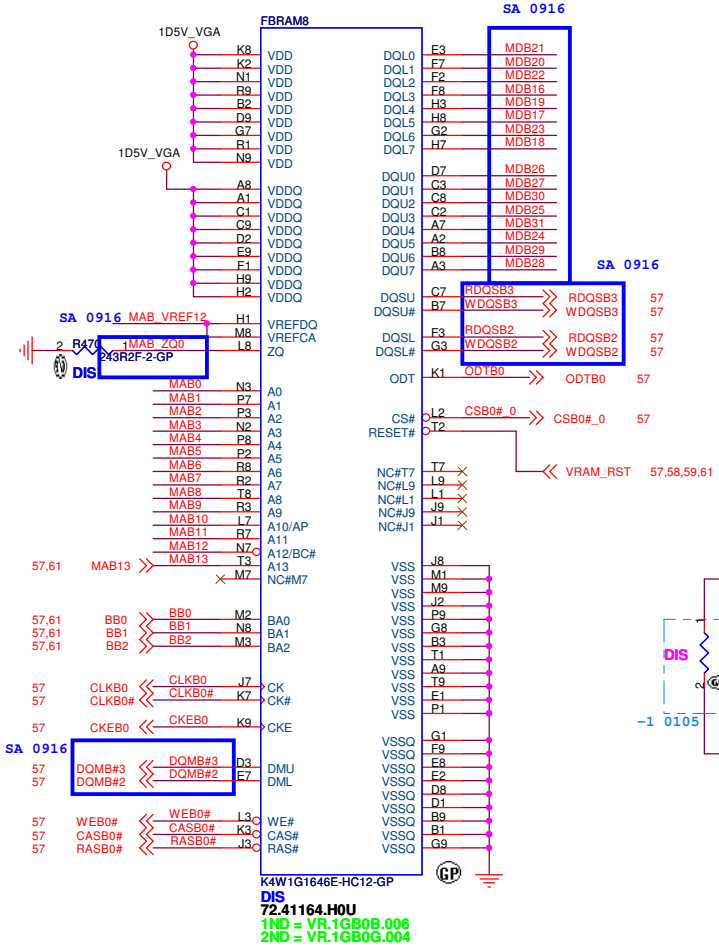
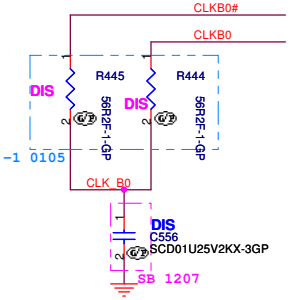
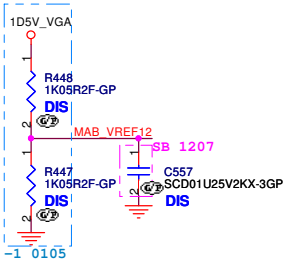
Title: VRAM(2/4)		
Size: A3	Document Number: JM31-CP	Rev: -1
Date: Thursday, February 25, 2010	Sheet 59 of 62	

DDR3









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HYNIX: 72.51G63.C0U(VR.1GB0G.004)

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57,61 RDQSB[0..7]
57,61 WDQSB[0..7]
57,61 MAB[0..12] MAB[0..12]
57,61 MDB[0..63] MDB[0..63]

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM(3/4)*

Size	Document Number	Rev
A3	JM31-CP	-1

Date: Thursday, February 25, 2010 Sheet 60 of 62

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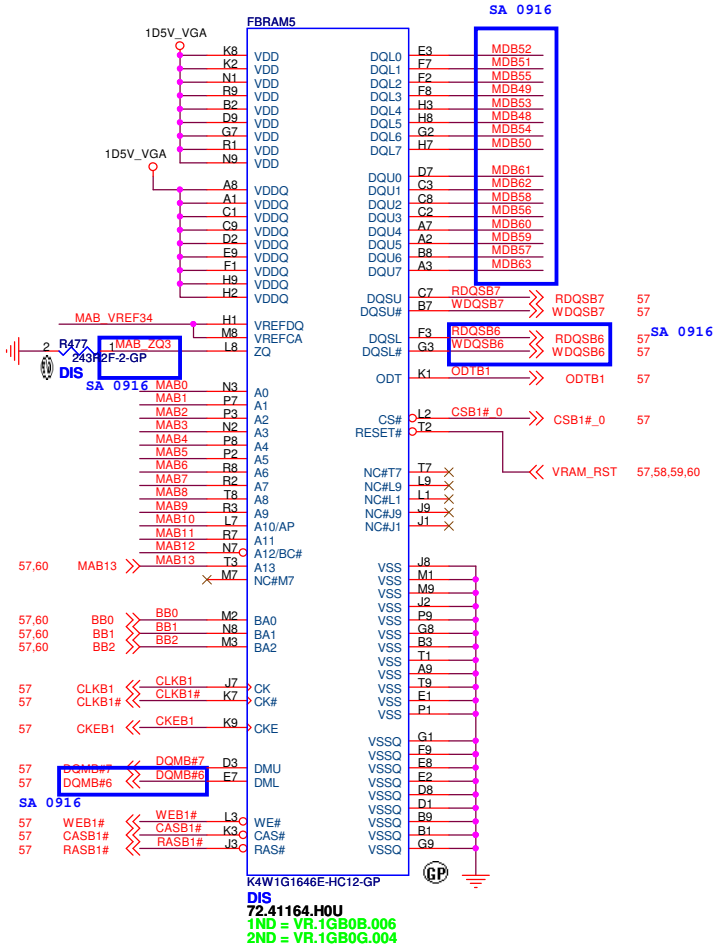
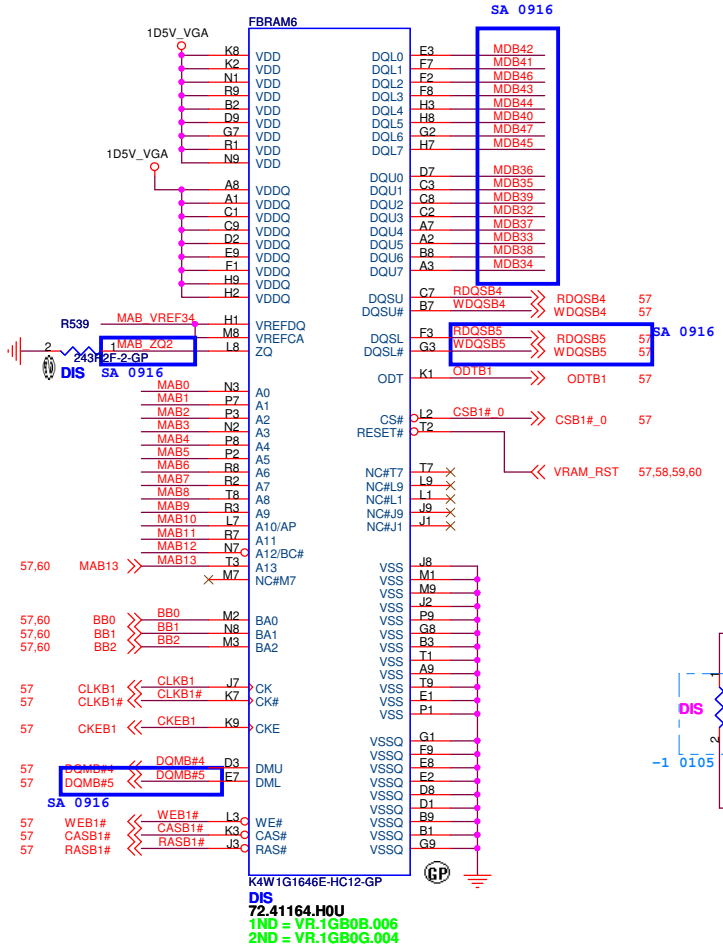
DDR3





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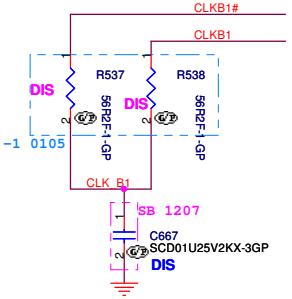

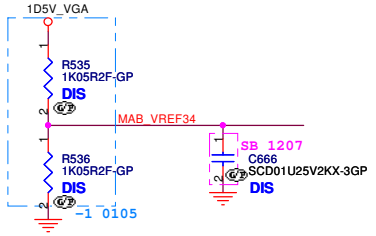

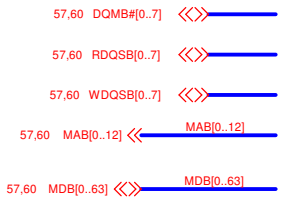

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Title: VRAM(4/4)		
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